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Electronic system specification language - Express information model VHDL 87

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REPORT

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English version

Electronic system specification languages Express information model VHDL 87

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European Committee for Electrotechnical Standardization
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Europäisches Komitee für Elektrotechnische Normung

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Foreword

This report, which contains an information model written in EXPRESS language[1)], was developed by Christian A. Giumale[2)] with support from both the ESIP project and the UK Defence Research Agency.

The model has been reviewed by a wide body of people from the VHDL community and presentations on this work have been given at VIUF in Washington and at an ESIP/CENELEC meeting hosted by Thomson in Paris.

The text of the report was approved by TC 217 on 1996-01-30 and approved for publication by the CENELEC Technical Board on 1996-07-02.

Background

The problems discussed in the present document resulted from work supported by the UK Defence Research Agency to produce a comprehensive information model of VHDL'87. As the research progressed it became clear that a single model of VHDL is not a satisfactory solution. Instead, a hierarchy of models, each of which describing the relevant aspects relating to a specific application purpose and from a specific perspective of VHDL, is a more satisfactory alternative. However, the model at the apex of this hierarchy describes the essential objects and the semantics of VHDL at the description, analysis, elaboration and simulation levels of design. It can be seen as an abstraction of all the other models in the hierarchy. Such a model, called here core model, and which is part of the present document, is a result of the above mentioned project.

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Support for the work described has been received from the UK Defence Research Agency and the Commission of the European Communities through the ESIP (ESPRIT 8370) project. We wish to thank in particular Andy Carpenter and Alan R. Williams (Manchester University UK), Jacques Rouillard (ESIM France), Serafin Olcoz and Juana Lopez (TGI Spain) for their useful comments and suggestions concerning modelling, VHDL modelling, and VHDL itself.

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1) EXPRESS Language reference manual ISO (DIS) 10303-11:1992, BSI.

2) University of Manchester, Oxford Road, Manchester M13 9PL UK

Contents

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Chapter 1

Information modelling of VHDL

The general aim of this chapter is to outline the power and the benefits which information modelling can provide to both the VHDL expert and the VHDL user according to the purpose of the model. More specifically, it is shown that (a) an information model of VHDL is worth considering as a viable alternative to other kinds models; (b) an information model can integrate different modelling goals and perspectives of VHDL more directly and uniformly; (c) an information model can be used to prove properties of the language, according to the model purpose; (d) there can be several VHDL information models depending on the goal of the model and the aspect of VHDL being considered and that these models can be organised into hierarchies for better support of complex applications, and (e) there are specific benefits of information modelling which can turn this paradigm into a valuable practical tool rather than a purely academic exercise. The discussion follows the plan shown below.

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In section 1.2 a short introduction to information modelling, using the EXPRESS language [ISO91] is presented. It is followed in section 1.3 by an example of individual VHDL object modelling which is the simplest stratum of a VHDL model. Section 1.4 shows that the core model has to consider transformation processes which interrelate different levels of VHDL design: description, analysis, elaboration and simulation and that the relevant features of these transformations can be conveniently modelled. Section 1.5 suggests the way the behavioural semantics of VHDL can be modelled. The three modelling goals discussed, individual object, cross-level modelling and behavioural modelling form a modelling space which is presented in section 1.6. In sections 1.7 and 1.9 the **core** model concept is presented and it is shown how a core model can be used to prove properties of the language. Section 1.8 presents the problem of hierarchies of models according to the purpose and the perspective of VHDL modelling. Finally the modelling purpose and benefits are considered.

The discussion which follows applies to VHDL'87, called VHDL hereafter. Note that for brevity the examples in this chapter are not meant to be complete.

1.1 Models of VHDL

VHDL [IE88] [IE93] is intended for use as a standard hardware design language in the microelectronic design community. It describes general digital hardware devices at an abstract level. The description is performed at the structural, behavioural and timing levels. An abstract event-driven simulation model is used to define the semantics of the language constructs by specifying the way they are evaluated while the simulation process unfolds.

There are many attempts to describe the VHDL semantics, particularly its behavioural semantics. The main purpose of these efforts is to capture in a clear and unambiguous notation what is described informally in the VHDL reference manual and then to use the resulting descriptions for different purposes such as the informal comparison of VHDL with other HDLs, the formal proof of properties of VHDL programs, the implementation of related