SLOVENSKI STANDARD
SIST ETS 300 337 E2:2003

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Prenos in multipleksiranje (TM) ï Generiļ ne strukture okvira za prenos razliļ nih signalov (vkljuļ no s celicami asinhronega prenosnega naļ ina (ATM) in elementi sinhrone digitalne hierarhije (SDH)) pri hierarhiļ nih hitrostih 2 048 kbit/s, 34 368 kbit/s in 139 264 kbit/s po priporoļ ilu ITU, G.702

Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s

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Foreword

This second edition European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS specifies generic frame structures for the transport of various signals at the ITU-T Recommendation G.702 [1] hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s. The support of Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) Tributary Units (TUs) in the Plesiochronous Digital Hierarchy (PDH) bit rates is also covered in this ETS.

This ETS takes into account the recommendations given in ITU-T Recommendation G.804 (annex B.2) and G.832 (annex B.3) - see annex B (Bibliography) for details.

Transposition dates	
Date of adoption:	7 March 1997
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1 Scope

This second edition European Telecommunication Standard (ETS) specifies generic frame structures for the transport of various signals at the ITU-T Recommendation G.702 [1] hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s. The support of Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) Tributary Units (TUs) in the Plesiochronous Digital Hierarchy (PDH) bit rates is covered in this ETS. Functions specific to the support of ATM cells performed in the transmitter and receiver are not part of this interface standard but are given for information in annex A.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] ITU-T Recommendation G.702 (1988): "Digital hierarchy bit rates".

[2] ETS 300 167: "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".

[3] ETS 300 147 (1995): "Transmission and Multiplexing (TM); Synchronous digital hierarchy; Multiplexing structure".

[4] ITU-T Recommendation G.831 (1996): "Management capabilities of transport networks based on the Synchronous Digital Hierarchy (SDH)".

[5] ITU-T Recommendation T.50 (1992): "Information technology - 7-bit coded character set for information interchange".

[6] ITU-T Recommendation G.707 (1995): "Synchronous Digital Hierarchy (SDH) bit rates".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of this ETS, the following definitions apply:

idle cell: A cell which is inserted and extracted by the adaptation function between the ATM virtual path layer network and the PDH path layer network in order to adapt the cell flow rate to the available payload capacity of the PDH path used.

valid cell: A cell whose header is declared by the cell Header Error Control (HEC) process to be free of errors.

NOTE: The order of transmission of information in all diagrams in this ETS is first from left to right and then top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left of all diagrams.

3.2 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

ATM	Asynchronous Transfer Mode
BIP-8	Bit Interleaved Parity - 8
CRC	Cyclic Redundancy Check
EM	Error Monitoring
FA	Frame Alignment
GC	General purpose Communication
HEC	Header Error Control
IEC	Incoming Error Count
MSB	Most Significant Bit
MA	Maintenance and Adaptation
NR	Network operatoR
OAM	Operations, Administration and Maintenance
PDH	Plesiochronous Digital Hierarchy
RDI	Remote Defect Indication
REI	Remote Error Indication
SDH	Synchronous Digital Hierarchy
SSM	Synchronization Status Message
TR	TRail trace
TS	Time Slot
TTI	Trail Trace Identifier
TU	Tributary Unit
TUG-n	Tributary Unit Group of level n
TU-x	Tributary Unit - x

4 Frame structure at 2 048 kbit/s

4.1 Basic frame structure

The basic frame structure at 2 048 kbit/s as described in ETS 300 167 [2] shall be used. This comprises a generic path overhead, a signalling channel and a generic payload capacity of 1 920 kbit/s.

4.2 Support of ATM cells in 2 048 kbit/s

Valid or idle cells are supported in bits 9 to 128 and bits 137 to 256 of the 2 048 kbit/s frame with the octet structure of the cells aligned with the octet structure of the frame (see figure 1). Bits 129 to 136 correspond to Time Slot 16 (TS 16) in an octet structured frame and are reserved for future use. Valid or idle cells occupy the whole of the payload and a cell can cross a 125 µs frame boundary. The ATM cell payload is scrambled using a self-synchronizing scrambler with the generator polynomial $x^{43} + 1$. Cell payload field scrambling is required to provide security against false cell delineation and to prevent the cell payload replicating the 2 048 kbit/s frame alignment word.

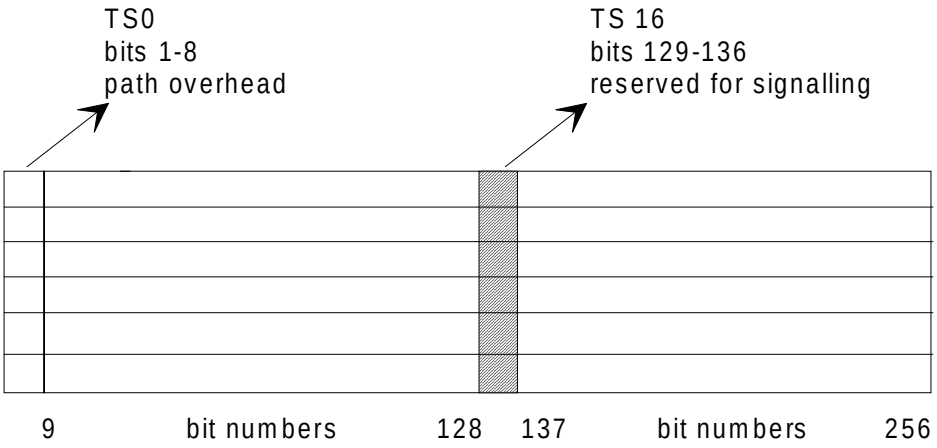

Figure 1: Frame structure at 2 048 kbit/s

5 Frame structure at 34 368 kbit/s

5.1 Basic frame structure

This frame structure is intended to be used in a generic way. When implementing this frame structure, care should be taken to ensure that the performance of the frame alignment mechanism is not compromised by the payload content.

5.1.1 General

The basic frame structure at 34 368 kbit/s comprises 7 octets of generic path overhead and 530 octets of payload capacity per 125 µs as shown in figure 2.

Figure 2: Frame structure at 34 368 kbit/s