TECHNICAL REPORT

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Information technology — Coding of audio-visual objects —

Part 9: Reference hardware description

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of the joint technical committee is to prepare International Standards. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

In exceptional circumstances, the joint technical committee may propose the publication of a Technical Report of one of the following types:

— type 1, when the required support cannot be obtained for the publication of an International Standard, despite repeated efforts;

— type 2, when the subject is still under technical development or where for any other reason there is the future but not immediate possibility of an agreement on an International Standard;

— type 3, when the joint technical committee has collected data of a different kind from that which is normally published as an International Standard ("state of the art", for example).

Technical Reports of types 1 and 2 are subject to review within three years of publication, to decide whether they can be transformed into International Standards. Technical Reports of type 3 do not necessarily have to be reviewed until the data they provide are considered to be no longer valid or useful.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

ISO/IEC TR 14496-9, which is a Technical Report of type 3, was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 29, *Coding of audio, picture, multimedia and hypermedia information*.

ISO/IEC TR 14496 consists of the following parts, under the general title *Information technology — Coding of audio-visual objects*:

— *Part 1: Systems*

— *Part 2: Visual*

— *Part 3: Audio*

— *Part 4: Conformance testing*

— *Part 5: Reference software*

— *Part 6: Delivery Multimedia Integration Framework (DMIF)*

— *Part 7: Optimized reference software for coding of audio-visual objects* [Technical Report]

— *Part 8: Carriage of ISO/IEC 14496 contents over IP networks*

— *Part 9: Reference hardware description* [Technical Report]

— *Part 10: Advanced Video Coding*

— *Part 11: Scene description and application engine*

— *Part 12: ISO base media file format*

— *Part 13: Intellectual Property Management and Protection (IPMP) extensions*

— *Part 14: MP4 file format*

— *Part 15: Advanced Video Coding (AVC) file format*

— *Part 16: Animation Framework eXtension (AFX)*

— *Part 17: Streaming text format*

— *Part 18: Font compression and streaming*

— *Part 19: Synthesized texture stream*

Introduction

The main goal of this Technical Report is to facilitate a more widespread use of the MPEG-4 standard.

Design methodologies of the EDA industry have evolved from schematics to Hardware Description Languages (HDLs) to address the needs of the vast number of gates available on a single device. The increased number of gates allowed more elaborate algorithms to be deployed but also required a shift in design paradigm to handle the complexity created. Through HDLs more complicated systems could be designed faster through the enabling technology of synthesis of the HDL code towards different silicon technologies where trade offs could be explored. Now the EDA industry again faces challenges where HDLs may not provide the level of abstraction needed for system designers to evaluate system level parameters and complexity issues. There have been a number of tool investigations under way to address this problem. Profiling tools aid in exposing bottlenecks in an abstract way so that early design decisions can be made. C to gates tools allow a C based simulation environment while also enabling direct synthesis to gates for hardware acceleration.

In conclusion, it is the aim of this Technical Report to enable more widespread use of the MPEG-4 standard through reference hardware descriptions and close integration with MPEG-4 Part 7 Optimized Reference Software. Additionally, it is aimed that exposure to such a platform will enable a more systematic way to investigate the complexity of new codecs and open up the algorithm search space with an order of magnitude more compute cycles.

Information technology — Coding of audio-visual objects —

Part 9:
Reference hardware description

1 Scope

This part of ISO/IEC 14496 specifies descriptions of the main video coding tools in hardware description language (HDL) form. Such alternative descriptions to the ones that are reported in ISO/IEC 14496-2, ISO/IEC 14496-5 and ISO/IEC TR 14496-7 correspond to the need of providing the public with conformant standard descriptions that are closer to the starting point of the development of codec implementations than textual descriptions or pure software descriptions. This part of ISO/IEC 14496 contains conformant descriptions of video tools that have been validated within the recommendation ISO/IEC TR 14496-7.

2 Copyright disclaimer for HDL software modules

Each HDL module has to be accompanied by the following copyright disclaimer that must be included in each HDL module and all derivative modules:


```
/*****************************************************************************

This software module was originally developed by
```



```
    <Family Name>, <Name>, <email address>, <Company Name>

    (date: <month>,<year>)

and edited by: <Family Name>, <Name>,<email address>

This HDL module is an implementation of a part of one or more MPEG-4
tools(ISO/IEC 14496).

ISO/IEC gives users of the MPEG-4 free license to this HDL module or
modifications thereof for use in hardware or software products claiming
conformance to the MPEG-4 Standard.

Those intending to use this HDL module in hardware or software products are
advised that its use may infringe existing patents.

The original developer of this HDL module and his/her company, the subsequent
editors and their companies, and ISO/IEC have no liability for use of this HDL
module or modifications thereof in an implementation.

Copyright is not released for non MPEG-4 Video conforming products.

<Company Name> retains full right to use the code for his/her own purpose, assign
or donate the code to a third party and to inhibit third parties from using the
code for non MPEG standard conforming products.
```

```
This copyright notice must be included in all copies or derivative works.

Copyright (c) <year>.

Module Name:  <module_name>.vhd

Abstract:


Revision History:

*****************************************************************/
```

3 Symbols and abbreviated terms

For the purposes of this document, the following symbols and abbreviated terms apply:

AV	Audio-Visual
DCT	Discrete Cosine Transform
IDCT	Inverse Discrete Cosine Transform
HDL	Hardware Description Language
ISO	International Organization for Standardization
MPEG	Moving Picture Experts Group
Verilog	A Hardware Description Language
VHDL	VHSIC high speed Hardware Description Language
SAD	Sum of Absolute Differences
MAC	Multiply ACcumulate
MAD	Minimum Absolute Difference
SIMD	Single Instruction Multiple Data
DA	Distributive Arithmetic
EDA	Electronic Design and Automation
IEEE	Institute of Electrical and Electronic Engineers
IMEC	Interuniversity Micro Electronic Center
EPFL	École Polytechnique Fédérale de Lausanne

4 HDL software availability

The HDL software modules described in this part of ISO/IEC 14496 are available within the zip file containing this Technical Report. Each module contains a separate directory structure for the source code with a readme.txt file explaining the top level and all files to be included for simulation and synthesis.

5 HDL coding format and standards

5.1 HDL standards and libraries

As the IEEE has several HDL coding standards that are commonly used in hardware reference code (i.e. VHDL1076-1987, VHDL 1164-1993, Verilog 1364-2000, Verilog 1364-1995), the modules constituting this part

of ISO/IEC 14496 are made of the latest IEEE standard possible at the time of coding for all reference HDL code. As the IEEE has provided libraries to assist in the use of HDL, only IEEE standard libraries are needed to use the HDL code.

Custom libraries which are specific to the vendor's (Silicon) base library elements are used only if they are freely available for synthesis and simulation and are provided in an accompanying module version of the submitted HDL code using the standard libraries mentioned above.

5.2 Conditions and tools for the synthesis of HDL modules

As there are many choices commercially for HDL synthesis and HDL simulation software tools, specific synthesis or simulation libraries that are used for reference HDL code are properly documented. The same code that is used to synthesize towards an implementation is also used to perform HDL behavioral simulation of the MPEG-4 tool. The code is properly documented with respect to the synthesis and simulation tool (and version) that has been used to perform the work. HDL module codes with multiple synthesis and simulation tools are also possible. In the event a source code modification must be made to support an additional synthesis or simulation tool, an additional source code is provided with proper documentation.

5.3 Conformance with the reference software

HDL reference code provides sufficient test bench code and documentation on how it is conformant with respect to the reference software. To the extent possible, bit and cycle true models are provided which can be used directly in the reference software code for verification. In the case that the reference HDL code is derived from other languages such as: C, C++, System C, Java, it is recommended that that this code and information on the methodology used to generate HDL should be provided to improve verification of conformance of the HDL code.

6 HDL modules

6.1 DCT/IDCT module Vers. 1

The aim of this module is to perform two dimensional Discrete Cosine Transform (DCT) and Inverse DCT (IDCT). The number of bits of the signed input data is limited to 12 bits for DCT and 16 bits for IDCT. The XN input represents the input data in row order 8×8 blocks. The XC output, after initial latency, will provide the DCT output data in signed format 16 bits with one fractional bit.

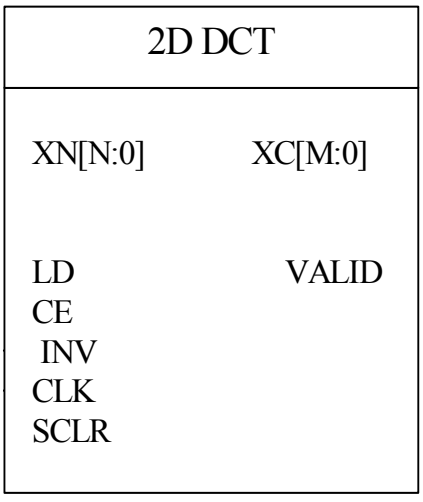

Figure 1 — The interface diagram of 2D DCT, 2D IDCT

Table 1 — Signals for 2D DCT — IDCT

Signal	Signal Direction	Description
XN[N:0]	Input	Block data in
LD	Input	Load data
INV	Input	DCT or IDCT
XC[M:0]	Output	(I)DCT data out
Valid	Output	Valid data on XC
CE	Input	Module enable
SCLR	Input	Module Reset
CLK	Input	Module Clock

Table 2 — Parameters for 2D DCT — IDCT

Parameter	Range
Width	N bits of input
Cwidth	12-20 coef bits for DCT coefs
Macwidth	32 internal multiply accumulate width
Intshift	2 bits internal shift in DCT
Intwidth	16 internal bits between stages of DCT
Oshift	0 bits of shift of the output data
Owidth	M bits of output from (I)DCT

6.1.1 Technical aspects of the algorithm and implementation

The two dimensional DCT is defined as:

$$DCTpq = \sum_{m=0}^{M-1}\sum_{n=0}^{N-1} BLKmn \cos\left(\frac{\pi(2m+1)p}{2M}\right)\cos\left(\frac{\pi(2n+1)q}{2N}\right)$$

For the use of DCT and IDCT in MPEG codecs the block size is 8 × 8 and thus M=N=8. In this implementation of the DCT a simple cascaded one dimensional approach is implemented. For the case of 8 × 8 block region this means that a one dimensional 8 point DCT on the rows is followed by internal double buffer memory and followed by another one dimensional 8 point DCT on the columns. The resultant complete architecture then provides the function of a two dimensional Discrete Cosine Transform.

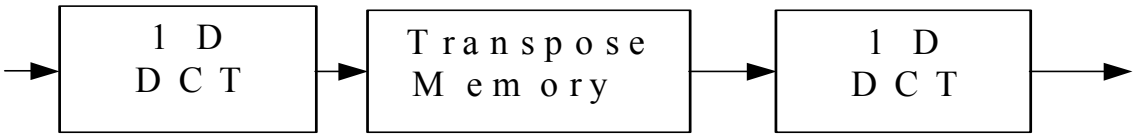

Figure 2 — The block diagram of the 2D DCT architecture

The implementation of the one dimensional DCT can be accomplished using a well known MAC technique with eight MACs, one for each DCT output. This approach has been investigated and shown to meet the performance criteria for video rate applications of MPEG.

6.2 Generic SAD engine for motion estimation

The aim of this module is to perform the sum of absolute differences (SAD) for a region of interest in the reference image given the current macroblock. The number of input bits is an input variable. The raster_in input signal represents the input data in row order. The motion vectors out are provided by mvx and mvy outputs and are signalled with the valid output. The actual value of the SAD is also given as an output so that a motion estimation algorithm may determine the minimum.

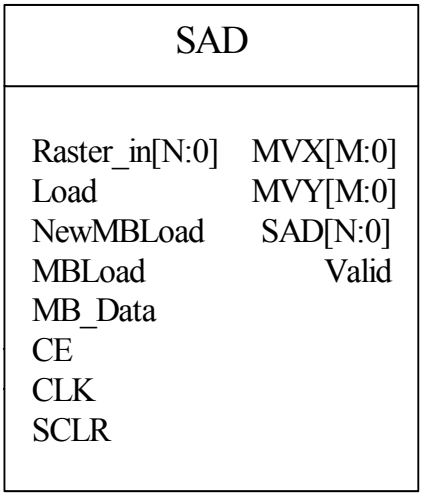

Figure 3 — SAD interface diagram