SLOVENSKI STANDARD
SIST EN 16602-60-02:2015

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Zagotavljanje varnih proizvodov v vesoljski tehniki - Razvoj vezij ASIC (aplikacijsko specifičnih IC) in FPGA (terensko programirljivih logičnih vezij)

Space product assurance - ASIC and FPGA development

Raumfahrtproduktsicherung - Entwicklung von ASIG und FPGA

Assurance produit des projets spatiaux - développement des ASIC et FPGA

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49.140	Vesoljski sistemi in operacije	Space systems and operations

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Space product assurance - ASIC and FPGA development

Assurance produit des projets spatiaux - développement des ASIC et FPGA

Raumfahrtproduktsicherung - Entwicklung von ASIG und FPGA

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Foreword

This document (EN 16602-60-02:2014) has been prepared by Technical Committee CEN/CLC/TC 5 “Space”, the secretariat of which is held by DIN.

This standard (EN 16602-60-02:2014) originates from ECSS-Q-ST-60-02C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

Introduction

The added responsibilities of developing custom designed devices, as opposed to using off-the-shelf components, make certain management activities crucial to the success of the procurement programme. This was already considered by the applicable standard for “Space product assurance - EEE components”, ECSS-Q-ST-60 that classifies custom designed devices, such as ASIC components, under “Specific components”, for which particular requirements are applicable.

The supplier accepts requirements for the development of custom designed components within the boundaries of this standard based on the requirements of the system and its elements, and takes into consideration the operational and environmental requirements of the programme.

The supplier implements those requirements into a system which enables to control for instance the technology selection, design, synthesis and simulation, layout and design validation in a schedule compatible with his requirements, and in a cost-efficient way.

1
Scope

This Standard defines a comprehensive set of requirements for the user development of digital, analog and mixed analog-digital custom designed integrated circuits, such as application specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs). The user development includes all activities beginning with setting initial requirements and ending with the validation and release of prototype devices.

This Standard is aimed at ensuring that the custom designed components used in space projects meet their requirements in terms of functionality, quality, reliability, schedule and cost. The support of appropriate planning and risk management is essential to ensure that each stage of the development activity is consolidated before starting the subsequent one and to minimize or avoid additional iterations. For the development of standard devices, such as application specific standard products (ASSPs) and IP cores, and devices which implement safety related applications, additional requirements can be included which are not in the scope of this document.

The principal clauses of this Standard correspond to the main concurrent activities of a circuit development programme. These include:

- ASIC and FPGA programme management,
- ASIC and FPGA engineering,
- ASIC and FPGA quality assurance.

The provisions of this document apply to all actors involved in all levels in the realization of space segment hardware and its interfaces.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system – Glossary of terms
EN 16602-10	ECSS-Q-ST-10	Space product assurance – Product assurance management
EN 16602-20	ECSS-Q-ST-20	Space product assurance – Quality assurance
EN 16602-30	ECSS-Q-ST-30	Space product assurance – Dependability
EN 16602-60	ECSS-Q-ST-60	Space product assurance – Electrical, electronic and electromechanical (EEE) components
EN 16603-10	ECSS-E-ST-10	Space engineering – System engineering general requirements
EN 16601-10	ECSS-M-ST-10	Space project management – Project planning and implementation
EN 16601-10-01	ECSS-M-ST-10-01	Space project management – Organization and conduct of reviews
EN 16601-40	ECSS-M-ST-40	Space project management – Configuration and information management

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 application specific integrated circuit (ASIC)

full custom or semi custom designed monolithic integrated circuit that can be digital, analog or a mixed function for one user

3.2.2 ASIC technology

totality of all elements required for the design, manufacture and test of ASIC components

NOTE Design tools and their description, cell libraries, procedures, design rules, process line and test equipment.

3.2.3 application specific standard products (ASSP)

ASICs designed to make standard products that are made available to a broader range of applications

NOTE ASSPs are most often are provided with a VHDL model and disseminated with documentation.

3.2.4 block diagram

abstract graphical presentation of interconnected named boxes (blocks) representing an architectural or functional drawing

3.2.5 cell

specific circuit function including digital or analog basic blocks

3.2.6 cell library

collection of all mutually compatible cells which conforms to a set of common constraints and standardized interfaces designed and characterized for a specified technology

3.2.7 data sheet

detailed functional, operational and parametric description of a component

NOTE A data sheet can include, for instance, a block diagram, truth table, pin and signal description, environmental, electrical and performance parameters, tolerances, timing information, and package description.

3.2.8 design flow

selection and sequence of engineering methods and tools to be applied during the implementation of the design

3.2.9 design for test (DFT) structure

technique used to allow a complex integrated circuit (IC) to be tested

NOTE This can include any mechanism aimed to provide better observability or commandability of internal nodes of the chip not accessible through primary inputs and outputs.

3.2.10 design iteration

design changes that occur in any single phase or between two consecutive phases as defined in the ASIC and FPGA development plan, before the design is released for prototype implementation

3.2.11 detail specification

procurement specification according to ESCC format that defines, for instance, the maximum ratings, parameter limitations, mechanical outline, pin description and screening requirements

3.2.12 development step

major step of the development flow for the ASIC and FPGA development

NOTE Definition phase, architectural design, detailed design, layout, prototype implementation and design validation.

3.2.13 fault coverage

measure expressed as a percentage of the proportion of actually detectable faults versus all possible faults in a digital circuit, for a given set of test patterns and with respect to a specific fault model

3.2.14 field programmable gate array (FPGA)

standard semiconductor device that becomes customized when programmed by the user with the FPGA specific software and hardware tools

3.2.15 floorplan

abstracted, scaled layout drawing of the die, outlining the form, size and position of the major functional blocks and the pads including power and ground lines, clock distribution and interconnect channels

3.2.16 HDL model

textual model based on a hardware description language (but not a piece of software in itself) suitable for the behavioural or structural description, simulation and by choosing a suitable level of abstraction for automatic netlist generation

3.2.17 intellectual property (IP) core

design element that implements a self-standing function or group of functions for which ownership rights exist

NOTE 1 IP core can be acquired by a customer, for a given price and under an owner-defined license agreement specifying the customer's acquired rights.

NOTE 2 IP core can be supplied as an HDL file (e.g. synthesizable VHDL code or gate-level netlist) and with the essential complementary documentation that allows the customer to successfully integrate and use it in a system (e.g. User's manual and verification files).

3.2.18 macrocell

module that contains complex functions in a manufacturer's cell library built up out of hard-wired primitive cells

3.2.19 netlist

formatted list of cells (basic circuits) and their interconnections

3.2.20 prototype device

fabricated ASIC or programmed FPGA used to validate the new design in respect to functionality, performance, operation limits and compatibility with its system

3.2.21 redesign

design changes which affect more than two consecutive phases of the ASIC and FPGA development or design changes that are implemented after prototype implementation

3.2.22 stimuli

input data set for simulation or test to show a specific functionality or performance of a device

3.2.23 test pattern

simulation stimuli and its expected responses (considering specific constraints to meet test equipment requirements) used to show correct behaviour of a device

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
ACP	ASIC and FPGA control plan
ADP	ASIC and FPGA development plan
ARS	ASIC and FPGA requirements specification
ASCII	American standard code for information interchange
ASIC	application specific integrated circuit
ASSP	application specific standard product
DD	design documentation
DDR	detailed design review
DFT	design for test
DRC	design rule check
DVP	design validation plan
EDA	electronic design automation
EDIF	electronic design interchange format
ERC	electrical rule check
ESCC	European Space Components Coordination
FM	flight module part
FPGA	field-programmable gate array
FRA	feasibility and risk analysis report
GDS	graphic design system (industry standard graphics entry tool)
HDL	hardware description language Note: This term used in general for the various hardware description language which are applied for coding during design phase such as VHDL and verilog.
IDMP	input data for mask or programming file generation
IEEE	Institute of Electrical and Electronics Engineers
IP	intellectual property
MoM	minutes of meeting
P&R	place and route
JTAG	joint test action group
LVS	layout vs. schematic check
NCC	netlist comparison check
QML	qualified manufacturer list
RTL	register transfer logic
SEU	single event upset
VHDL	VHSIC hardware description language