SLOVENSKI STANDARD
SIST EN 16602-60-12:2015

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Zagotavljanje varnih proizvodov v vesoljski tehniki - Snovanje, izbiranje, nabava in uporaba monolitnih mikrovalovnih integriranih vezij (MMIC) v obliki čipov

Space product assurance - Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs)

Raumfahrtproduktsicherung - Design, Auswahl, Beschaffung und Nutzung von MMIC

Assurance produit des projets spatiaux - Conception, sélection, approvisionnement et utilisation de circuits intégrés monolithique hyperfréquence de forme die

Ta slovenski standard je istoveten z: **EN 16602-60-12:2014**

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English version

Space product assurance - Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs)

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Table of contents

Figures

Tables

Foreword

This document (EN 16602-60-12:2014) has been prepared by Technical Committee CEN/CLC/TC 5 “Space”, the secretariat of which is held by DIN.

This standard (EN 16602-60-12:2014) originates from ECSS-Q-ST-60-12C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

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Introduction

This Standard covers the design, selection, procurement and use of III-V monolithic microwave integrated circuits (MMICs) for space equipment.

It defines the design activity for the technical (methodology, phases to be followed) and quality (quality assurance, design review) aspects, and, the selection and procurement rules for these components taking into account whether or not the processes have been validated.

1
Scope

This Standard applies to all types of MMIC (monolithic microwave integrated circuit) based on III-V compound materials for RF applications (i.e. frequency range ≥ 1 GHz). The requirements for the procurement of components in die form are defined.

It is not within the scope of this Standard to address packaged MMICs and discrete microwave components, these are dealt with in the relevant ESCC specification (ESCC 9010 and ESCC 5010).

This standard may be tailored for the specific characteristic and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system – Glossary of terms
EN 16602-30-11	ECSS-Q-ST-30-11	Space product assurance — Derating -- EEE components
EN 16602-60	ECSS-Q-ST-60	Space product assurance - Electrical, electronic and electromechanical (EEE) components
EN 16602-60-05	ECSS-Q-ST-60-05	Space product assurance — Generic requirements for hybrids
	MIL-STD-883	Tests methods and procedures for microelectronics
	ESCC 20600	Preservation, packaging and despatch of ESCC electronic components
	ESCC 24600	Minimum quality management system requirements
	ESCC 2049010	Internal visual inspection of monolithic microwave devices
	ESCC 2439010	Requirements for capability approval of MMICs
	ESCC 9010	Generic specification for MMICs

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this document, the terms and definitions given in ECSS-S-ST-00-01 apply.

For the purpose of this document, the following term from ECSS-Q-ST-60-05 applies:

process identification document

3.2 Terms specific to the present document

3.2.1 batch lot

wafers from the same basic raw materials processed as a single set in the manufacturing sequence (diffusion, metallization and passivation process) in a limited and controlled period of time

NOTE A unique identifier or code is assigned to a batch lot and to each wafer for processing traceability purposes.

3.2.2 design rules check

control procedure for verifying that design rules have been satisfied

NOTE 1 Design rules checks are generally issued by the supplier.

NOTE 2 DRC is performed using software.

3.2.3 designer

organization responsible for the design of the MMICs

3.2.4 die lot

set of all dies coming from a single wafer lot

3.2.5 electrical rule check

control procedure for verifying that the electrical rules have been satisfied

NOTE Electrical rules are generally issued by the manufacturer.

3.2.6 evaluated process

mature technology that has been successfully submitted to a set of electrical and environmental testing to demonstrate performance and reliability limits

NOTE 1 ECSS-Q-ST-60-01 contains a list of evaluated processes.

NOTE 2 The ESCC 2269010 specification defines the requirements for the evaluation.

3.2.7 manufacturer

foundry responsible for the manufacturing of the MMICs

3.2.8 process control monitor

test vehicle used by the supplier to assess the stability of the manufacturing process by means of controls conducted during a wafer production cycle

NOTE The PCM is repeated a number of times (depending on the manufacturers) on each wafer lot. The measurements taken during the PCM are used to accept or reject the wafer according to the relevant DC and RF criteria defined in the design manual.

3.2.9 production lot

device types manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment

NOTE A production lot may be composed of one or many batch lots.

3.2.10 qualified process

process that has been successfully submitted to a formal qualification testing

NOTE The ESCC 20100 specification defines the requirements for the qualification.

3.2.11 reticule

group of circuit layouts (MMIC, TCV, DEC, PCM) defined by design at the mask level, for duplication over the entire wafer during the MMIC manufacturing

3.2.12 statistical process control

tool to control the quality and the stability of the technological process

NOTE SPC is implemented by measuring key parameters during the different manufacturing steps and their analysis using appropriate methods.

3.2.13 tile

See **reticule**

3.2.14 user

entity responsible for the integration of the MMICs at upper level

NOTE Example: MMICs are integrated by users into, for example, modules, hybrids, piece of equipment.

3.2.15 validated design

design that is successfully submitted to application approval testing and an MMIC user LAT test

3.2.16 validated process

process that is evaluated or qualified

3.2.17 wafer lot

wafers manufactured from one or more batch lots

NOTE Depending on the maturity of the process a wafer lot is defined as follows:

- Case 1 (non-evaluated or qualified process): a wafer lot is a single wafer.
- Case 2 (evaluated or qualified process and new MMIC design): a wafer lot is one batch lot.
- Case 3 (mature process and recurrent MMIC design): a wafer lot is considered to be a production lot of 4 batches manufactured within a 3 month period.

3.3 Abbreviated terms

For the purpose of this standard, the abbreviated terms of ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AQL	acceptance quality level
CTA	circuit type approval
DEC	dynamic evaluation circuit
DRC	design rules check
ERC	electrical rule check
HTRB	high-temperature reverse bias
LAT	lot acceptance test
LTRB	low-temperature reverse bias
MMIC	monolithic microwave integrated circuit
PAD	part approval document
PCM	process control monitor
PID	process identification document

RGA	residual gas analysis
SAM	scanning acoustic microscopy
SEM	scanning electron microscope
SEU	single event upset
SPC	statistical process control
TCV	technological characterization vehicle
WAT	wafer acceptance testing