

SLOVENSKI STANDARD SIST EN 16602-70-28:2015

01-januar-2015

Zagotavljanje varnih proizvodov v vesoljski tehniki - Popravilo in spreminjanje plošč tiskanih vezij za vesoljsko uporabo

Space product assurance - Repair and modification of printed circuit board assemblies for space use

Raumfahrtproduktsicherung - Reparatur und Modifikation von Leiterplatten-Baugruppen für den Einsatz im Weltraum STANDARD PREVIEW

Assurance produit des projets spatiaux - Réparation et modification des ensembles de circuits imprimés pour utilisation spatiale, 16602-70-28:2015

https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-

Ta slovenski standard je istoveten z: EN 16602-70-28-2015

ICS:

31.180 Tiskana vezja (TIV) in tiskane Printed circuits and boards

plošče

49.140 Vesoljski sistemi in operacije Space systems and

operations

SIST EN 16602-70-28:2015 en

SIST EN 16602-70-28:2015

iTeh STANDARD PREVIEW (standards.iteh.ai)

SIST EN 16602-70-28:2015

https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-2a9f914a46d2/sist-en-16602-70-28-2015

EUROPEAN STANDARD NORME EUROPÉENNE EUROPÄISCHE NORM EN 16602-70-28

October 2014

ICS 49.140

English version

Space product assurance - Repair and modification of printed circuit board assemblies for space use

Assurance produit des projets spatiaux - Réparation et modification des ensembles de circuits imprimés pour utilisation spatiale

Raumfahrtproduktsicherung - Reparatur und Modifikation von Leiterplatten-Baugruppen für den Einsatz im Weltraum

This European Standard was approved by CEN on 11 April 2014.

CEN and CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration. Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CEN and CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CEN and CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CEN and CENELEC members are the national standards bodies and national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and United Kingdom.

2a9f914a46d2/sist-en-16602-70-28-2015





CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

Table of contents

Forew	ord	9
1 Sco	pe	10
2 Norı	mative references	11
3 Terr	ns, definitions and abbreviated terms	12
3.1	Terms from other standards	12
3.2	Terms specific to the present standard	12
3.3	Abbreviated terms	13
4 Req	uirements	14
4.1	Basic requirementsS.T.A.N.D.A.R.DP.R.E.V.III.W	14
	4.1.1 Hazard, health and safety precautions	14
	4.1.1 Hazard, health and safety precautions	14
	4.1.3 Facilities <u>SIST EN 16602-70-28:2015</u>	
	4.1.4 https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4- General2a9f914a46d2/sist-en-16602-70-28-2015	14
4.2	Repairs	
	4.2.1 Repair criteria	15
	4.2.2 Number of repairs	15
4.3	Modifications	15
	4.3.1 Modification criteria	15
	4.3.2 Number of modifications	16
4.4	Rework	16
	4.4.1 Rework criteria	16
	4.4.2 Number of reworks	16
4.5	Other requirements	16
4.6	Removal of conformal coating	
	4.6.1 Requirements	
	4.6.2 Procedure	
	4.6.3 Acceptance criteria	
4.7	Solder joint removal and unclinching	
	4.7.1 Procedure	

	4.7.2	Acceptance criteria	18
4.8	Repair o	of damaged gold-plated areas	18
	4.8.1	Requirements	18
	4.8.2	Procedure	18
	4.8.3	Acceptance criteria	19
4.9	Repair o	of damaged conductor tracks	19
	4.9.1	Requirements	19
	4.9.2	Procedure	19
	4.9.3	Acceptance criteria	20
4.10	Repair o	of lifted conductors	20
	4.10.1	Requirements	20
	4.10.2	Procedure	20
	4.10.3	Acceptance criteria	20
4.11	Repair o	of lifted terminal areas (pads)	21
	4.11.1	Requirements	21
	4.11.2	Procedure	21
	4.11.3	Acceptance criteria	21
4.12	Termina	al post replacement	21
	4.12.1	Requirements	21
	4.12.2	ProcedureSIST.EN.16602-70-28:2015	
	4.12.3	https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-Acceptance criteria 446d2/sist-en-16602-70-28-2015	21
4.13	Wire-to-	wire joints	
	4.13.1	Requirements	22
	4.13.2	Procedure	22
	4.13.3	Acceptance criteria	22
4.14	Addition	of components	22
	4.14.1	Requirements	22
	4.14.2	Procedure	23
	4.14.3	Acceptance criteria	23
4.15	Remova	al and replacement of axial and multi-lead components	24
	4.15.1	Requirements	24
	4.15.2	Procedure	24
	4.15.3	Acceptance criteria	24
4.16	Remova	al and replacement of flat-pack components	24
	4.16.1	Requirements	24
	4.16.2	Procedure	24
	4.16.3	Acceptance criteria	25

4.17	Modific	ation of component connections	25
	4.17.1	Requirements	25
	4.17.2	Procedure	25
	4.17.3	Acceptance criteria	26
4.18	Cutting	of internal track of a multi-layer printed circuit board	26
	4.18.1	Procedure	26
	4.18.2	Acceptance criteria	26
4.19	Quality	assurance	26
	4.19.1	General	26
	4.19.2	Data	26
	4.19.3	Nonconformance	27
	4.19.4	Calibration	27
	4.19.5	Traceability	27
	4.19.6	Operator and inspector training and certification	27
Annex	A (info	rmative) Removal of conformal coating	28
A.1		ction	
A.2	Tools a	nd materials STANDARD PREVIEW	28
A.3	Method	ls for the removat of conformat coating have in	28
	A.3.1	Method for the removal of polyurethane and silicone-type coating	28
	A.3.2	SIST EN 16602-70-28:2015 Method for the removal of epoxy-type coating 3-4c45-a2c4-	29
Annex	B (info	2a9f914a46d2/sist-en-16602-70-28-2015 rmative) Solder joint removal and unclinching	
B.1	-	ction	
B.2	Tools a	nd materials	31
B.3	Method	ls for solder joint removal and unclinching	31
	B.3.1	Method for solder extraction with continuous vacuum	
	B.3.2	Method for solder extraction using sucker	
	B.3.3	Method for hot jet extraction	
	B.3.4	Method for the use of wicking braid	33
	B.3.5	Method for unclinching of leads	34
Annex	C (info	rmative) Repair of damaged gold-plated areas	35
C.1	Introdu	ction	35
C.2	Tools and materials		
C.3	Method	ls for the repair of damaged gold-plated areas	35
	C.3.1	Method for the removal of solder splatter on gold plating	35
Annex	D (info	rmative) Repair of damaged conductor tracks	36
D.1	Introdu	ction	36

D.2	Tools ar	nd materials	36	
D.3	Method for the repair of damaged conductor tracks			
Annex	E (infor	mative) Repair of lifted conductors	37	
E.1				
E.2	Tools ar	nd materials	37	
E.3	Methods	s for repair of lifted conductors	38	
	E.3.1	Method for the use of epoxy under conductor	38	
	E.3.2	Method for the use of epoxy over conductor	38	
Annex	F (infor	mative) Repair of lifted terminal areas (pads)	39	
F.1	Introduc	etion	39	
F.2	Tools ar	nd materials	40	
F.3	Method	for the repair of lifted terminal areas (pads)	40	
Annex	G (info	rmative) Terminal post replacement	41	
G.1	Introduc	tion	41	
G.2	Tools and materials			
G.3	Method for the replacement of terminal post .P.R.F.V.I.F.W			
Annex	H (infor	mative) Wire-to-wire jointss.iteh.ai)	43	
H.1	Introduc	stion <u>SIST EN 16602-70-28:2015</u>	43	
H.2	Tools ar	nd Impaterials rds.itch.ai/catalog/standards/sist/935badf0-7693-4c45-a2c4	43	
H.3	Method	for wire-to-wire joining dd2/sist-en-16602-70-28-2015	43	
Annex	l (inforr	native) Addition of components	45	
I.1	Introduc	etion	45	
1.2	Tools ar	nd materials	45	
1.3	Methods	s for addition of components	46	
	I.3.1	Method for additional components mounted on reverse (non-component) side of board	46	
	1.3.2	Method for additional components mounted on component side of board	47	
	1.3.3	Method for additional components mounted on terminal posts, including "piggyback" mounting	48	
	1.3.4	Method for additional components mounted (on reverse side or on component side of board) using staking compound	49	
	1.3.5	Method for additional components mounted (on reverse side or on component side of board) to leads of adjacent components	50	
	1.3.6	Method for the addition of a wire link onto soldered chips on a single side piece of PCB with appropriate pads	55	
	1.3.7	Method for the addition of a wire link onto metallized cap of chips directly glued on PCB	56	

		rmative) Removal and replacement of axial and multi-lead	6 7
	-	ts	
J.1		uction	
J.2		and materials	
J.3	Method	ds for removal and replacement of axial and multi-lead components	57
	J.3.1	Method for the removal of components with axial leads (destructive removal)	57
	J.3.2	Method for the removal of multi-lead components (destructive removal)	58
Annex	K (info	ormative) Removal and replacement of flat-pack components	60
K.1	Introdu	uction	60
K.2	Tools a	and materials	60
K.3	Method	d for the removal and replacement of flat-pack components	60
Annex	L (info	ormative) Modification of component connections	62
L.1	Introdu	uction	62
L.2	Tools a	and materials	62
L.3	Method	ds for modification of component connections	62
	L.3.1	Method for the soldering of a wrap-around connection to an extended component lead Landard S. Iteh. al.	
	L.3.2	Method for the soldering of component lead to a stud lead mounted into an existing hole https://standards.iteh.a/catalog/standards/sist/935badf0-7693-4e45-a2c4-	63
	L.3.3	Method for mounting a dual-in-line (DIL) package with or without a wire link soldered onto a cropped lead	
	L.3.4	Method for mounting a connector with or without a wire link soldered onto a cropped lead	66
	L.3.5	Method for the addition of a wire link into a plated-through hole occupied by a flat-section lead	67
	L.3.6	Method for the addition of a wire link on top of a flat-pack lead	69
	L.3.7	Method for the isolation of a component lead	69
	L.3.8	Method for the addition of a wire link onto terminal pad of soldered chips	71
		ormative) Cutting of internal track of a multi-layer printed	73
M.1		ıction	
M.2	Tools and materials		
M.3	Method for cutting the internal track of a multi-layer printed circuit board		
Biblio	graphy.		75

Figures

Figure A-1 : Removal of coating by thermal parting device	30
Figure B-1 : Continuous vacuum solder extraction on stud lead	32
Figure B-2 : Pulse-type solder sucker in use	32
Figure B-3 : Lifting individual leads with hot jet	33
Figure B-4 : Cross-sectional view of wicking method	34
Figure B-5 : Hot unclinching with thermal parting device	34
Figure E-1 : Lifted conductors	37
Figure E-2 : Repair using epoxy under conductor	38
Figure E-3 : Repair using epoxy over conductor	38
Figure F-1 : Lifted terminal area	39
Figure F-2 : Terminal areas without track	39
Figure F-3 : Terminal areas with track attached	40
Figure G-1 : Terminal post replacement	42
Figure H-1 : Use of approved type support clamp/heat sink	44
Figure I-1: Additional components mounted on reverse (non-component) side of b	oard47
Figure I-2 : Additional components mounted on component side of board	48
Figure I-3: "Piggyback" mounting of one component on top of another	
Figure I-4: Mounting and wiring of additional axially-leaded components mounted reverse side or on component side of board) using staking compound.	
Figure I-5 : Upside down mounting and wiring of additional side brazed DIL compo (on reverse side or on component side of board) using staking compou	
Figure I-6: Mounting of additional non-axially leaded components, e.g. capacitors, wire connecting top or bottom sides of the circuit board using staking compound (on reverse side or on component side of board)	
Figure I-7: Mounting of additional component (on component side of board) with w connections on reverse side of board using staking compound	vire 53
Figure I-8: Mounting of additional component (on reverse side of board) across extended leads of adjacent components	53
Figure I-9 : Mounting of additional component by linking to a "pigtailed" lead of an adjacent component	54
Figure I-10: Mounting of additional component by linking to lead of an adjacent transistor (or other large component)	55
Figure I-11: Addition of a wire link onto metallized cap of chips directly glued on P	CB56
Figure J-1 : Removal of multi-lead components, clipping of component leads	58
Figure J-2: Removal of multi-lead components, removal of remaining component I	eads59
Figure K-1 : Removal of flat-pack components	61
Figure L-1 : Soldering of a wrap-around connection to an extended component lea	d63
Figure L-2: Soldering of component lead to a stud lead mounted into an existing h	ole64

Figure L-3: Mounting a dual-in-line package with or without a wire link soldered onto a cropped lead (cropped lead without connection and cropped lead with connection led through hole and onto board)	65
Figure L-4: Mounting a dual-in-line package with or without a wire link soldered onto a cropped lead (wire link passing away from board)	66
Figure L-5: Mounting a connector with a wire link soldered onto a cropped lead	67
Figure L-6 : Addition of a wire link into a plated through hole occupied by a flat-section lead (wire link entering from the reverse side of the board)	68
Figure L-7 : Addition of a wire link into a plated through hole occupied by a flat-section lead (wire link entering from the component side of the board)	68
Figure L-8 : Addition of a wire link on top of a flat-pack lead	69
Figure L-9 : Isolation of a component lead	71
Figure L-10 : Addition of a wire link onto terminal pad of soldered chips	72
Figure M-1 : Cutting of internal track of a multi-layer circuit board	74
Tables	
Table 4-1: Wire diameters for given conductor widths	19

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>SIST EN 16602-70-28:2015</u> https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-2a9f914a46d2/sist-en-16602-70-28-2015

Foreword

This document (EN 16602-70-28:2014) has been prepared by Technical Committee CEN/CLC/TC 5 "Space", the secretariat of which is held by DIN.

This standard (EN 16602-70-28:2014) originates from ECSS-Q-ST-70-28C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by April 2015, and conflicting national standards shall be withdrawn at the latest by April 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g., raerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

1 Scope

The requirements and procedures for repair and modification detailed in this Standard are designed to maintain the rigorous standards set by the customer for the manufacture and assembly of space-quality printed circuit boards.

This Standard is confined to the repair and modification of single-sided, double-sided and multi-layer printed circuit board assemblies.

This Standard does not address the potential need for rework resulting from a repair or modification and unassembled (bare) printed circuits boards.

This standard may be tailored for the specific characteristics and constraints of a space project, in conformance with ECSS-S-ST-00.

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>SIST EN 16602-70-28:2015</u> https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-2a9f914a46d2/sist-en-16602-70-28-2015

Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies

EN reference	Reference in text	Title
EN 16001-00-01	ECSS-S-ST-00-01	ECSS system — Glossary of terms
EN 16602-10-09	ECSS-Q-ST-10-09 (stand	Space product assurance — Nonconformance control system 1161.21)
EN 16602-20	ECSS-Q-ST-20	Space product assurance — Quality assurance
EN 16602-70	ht ECSS+Q+ST+70 h.ai/catalog/ 2a9f914a46d2/	
EN 16602-70-08	ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high-reliability electrical connections
EN 16602-70-10	ECSS-Q-ST-70-10	Space product assurance — Qualification of printed circuit boards
EN 16602-70-38	ECSS-Q-ST-70-38	Space product assurance — High-reliability soldering for surface-mount and mixed technology

3

Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 modification

process of modifying an electronic circuit by means of the addition or removal of electrical parts or wiring RD PREVIEW

3.2.2 (repaindards.iteh.ai)

change of a component with all its associated connections, including the fixing down of a lifted pad or tracks of any similar procedure described in this Standard 2a9f914a46d2/sist-en-16602-70-28-2015

NOTE 1 Changing of components for tuning, i.e. de-soldering and changing component value is not considered a repair, rework or modification operation.

NOTE 2 During tuning, solder jointing is achieved with a minimum of solder, just enough to ensure contact.

3.2.3 rework

process of reworking of a defective solder joint (without component changing) as a consequence of the repair or modification process or for restoring good workmanship of potentially defective solder joints

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
PCB	printed circuit board
PTFE	Polytetrafluoroethylene
PTH	plated-through hole
DIL	dual-in-line

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>SIST EN 16602-70-28:2015</u> https://standards.iteh.ai/catalog/standards/sist/935badf0-7693-4e45-a2c4-2a9f914a46d2/sist-en-16602-70-28-2015