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### **Foreword**

This Technical Report (TR) has been produced by ETSI Technical Committee Smart Card Platform (SCP).

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- the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, y: updates, etc.
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The aim was to develop a technical report (TR) that defines how to optimally set up the test environment to execute test case implementations based on ETSI TC SCP test specifications.

# Modal verbs terminology

In the present document "shall", "shall not", "should", "should not", "may", "need not", "will", "will not", "can" and "cannot" are to be interpreted as described in clause 3.2 of the ETSI Drafting Rules (Verbal forms for the expression of provisions).

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#### 1 Scope

The present document provides how to optimally set up the test environment to execute test case implementations based on ETSI TC SCP test specifications.

This includes (but is not limited to):

- Derived guidelines to set up a test environment;
- Test equipment behaviour in case of additional activity triggered by test sequences;
- Optimization of the test environment;
  - Noise issues when using the Single Wire Protocol;
  - Limiting the noise impacts;
- Checking the integrity of the test environment;
- Example of a Test Case for Integrity check.

The targeted audience for the present document is users of test case implementations based on ETSI TC SCP test specifications as well as test equipment manufacture.

#### 2 References

#### Normative references 2.1

2.1 Normative references

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The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

- ETSI TS 102 613: "Smart Cards; UICC Contactless Front-end (CLF) Interface; Part 1: Physical [i.1] and data link layer characteristics".
- [i.2] ETSI TS 102 694-1: "Smart Cards; Test specification for the Single Wire Protocol (SWP) interface; Part 1: Terminal features".

- [i.3] ETSI TS 102 221: "Smart Cards; UICC-Terminal interface; Physical and logical characteristics".
- [i.4] ISO/IEC 14443-4: "Identification cards Contactless integrated circuit(s) cards Proximity cards Part 4: Transmission protocol".

# 3 Definitions, symbols and abbreviations

### 3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

card emulation mode: mode where the UICC emulates a contactless card through the CLF

class A operating conditions: terminal or a smart card operating at 5 V  $\pm$  10 %

class B operating conditions: terminal or a smart card operating at 3 V  $\pm$  10 %

class C operating conditions: terminal or a smart card operating at 1,8 V  $\pm$  10 %

contactless frontend: circuitry in the terminal which:

- handles the analogue part of the contactless communication;
- handles communication protocol layers of the contactless transmission link;
- exchanges data with the UICC.

full duplex: simultaneous bidirectional data flow

half duplex: sequential bidirectional data flow

idle bit: bit with logical value 0 sent outside a frame

master: entity which provides the \$1 signal

reader mode: mode where the UICC act as a contactless reader through the CLF

state H: high electrical level of a signal (voltage or current)

state L: low electrical level of a signal (voltage or current)

**S1:** signal from the master to a slave

**S2:** signal from the slave to the master

slave: entity which is connected to the master and provides the S2 signal

**transition sequence:** signal sent by the master during *RESUME*, consisting of the falling edge, the state L period and the rising edge of an idle bit

ETSI TS 102 221 [i.3] interface: asynchronous serial UICC-Terminal interface defined in ETSI TS 102 221 [i.3], using RST on contact C2, CLK on contact C3 and I/O on contact C7

#### **UICC** powering modes:

- **full power mode:** The UICC is powered according to ETSI TS 102 221 [i.3] limitations in operating state.
- low power mode: The UICC is running in a reduced power mode as defined in the present specification.

## 3.2 Symbols

For the purposes of the present document, the following symbols apply:

Gnd Ground

I<sub>H</sub> Current signalling state H of S2

Current signalling state L of S2  $I_{L}$ 

T Bit duration

 $T_{H1}$ Duration of the state H for coding a logical 1 of S1  $T_{H0}$ Duration of the state H for coding a logical 0 of S1 Processing time of the CLF for a packet of data  $T_{CLF}$ 

Transfer time of contactless command or response over the RF interface  $T_{RFn}$ 

 $T_{SWP}$ Transfer time a single SWP packet of date

Processing time of the UICC for a contactless command  $T_{UICC}$ 

Fall time Rise time  $t_R$ Vcc Supply Voltage Input Voltage (high)  $V_{IH}$ Input Voltage (low)  $V_{IL}$  $V_{OH}$ Output Voltage (high)  $V_{OL}$ Output Voltage (low)

#### 3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

**ACT CLF** 

**CLK** 

**DUT** 

**FSC** 

**HDLC** 

I/O

Input/Output
International Organization for Standardization
Near Field Communication - Interface and Processing Proximity Coupling Device
Radio Frequency
ReseT
Implified History ISO NFCIP-1

**PCD** 

RF

**RST** 

**SHDLC** Single Wire protocol Input/Output **SWIO** 

Single Wire Protocol Universal Serial Bus **SWP USB** 

### 4 Optimization of the test environment for terminal testing using the Single Wire Protocol

#### Noise issues when using the Single Wire Protocol 4.1

As a reminder, here is the description of the principle of the Single Wire Protocol.

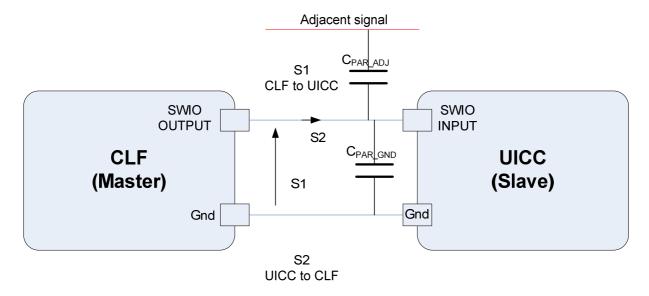


Figure 4.1: SWP data transmission

The principle of the Single Wire Protocol is based on the transmission of digital information in full duplex mode:

- The signal S1 is transmitted by a digital modulation (L or H) in the voltage domain.
- The signal S2 is transmitted by a digital modulation (O or H) in the current domain.

Since S2 is in the current domain, the immunity to noise is unfortunately quite low.

There are indeed several contributors to the current carried over SWIO (called ITOT):

- 1) Obviously S2 signal, intentionally generated by the UICC;
- 2) **I**<sub>CAP-GND</sub>, which is the current necessary to charge (discharge) the SWIO line parasitic capacitance to ground (C<sub>PAR-GND</sub> as drawn on figure 4.1): indeed, C<sub>PAR-GND</sub> has to be charged (discharged) each time S1 presents a rising (falling) edge. This noise is therefore synchronous with S1 and can then be removed from I<sub>TOT</sub> by the CLF which knows when these edges take place;
- 3) **I**<sub>CAP-ADJ</sub>, which is the current necessary to charge (discharge) the SWIO line parasitic capacitance to a signal adjacent to SWIO (C<sub>PAR\_ADJ</sub> as drawn on figure 4.1): unlike I<sub>CAP-GND</sub>, I<sub>CAP-ADJ</sub> is only partially synchronous with S1 transitions: in addition to the current required to charge I<sub>CAP-ADJ</sub> when there is an edge on S1, there are additional parasitic current pulses on I<sub>CAP-ADJ</sub> created by the transition which occur on the adjacent signal and which are very likely asynchronous with S1 transitions. These asynchronous pulses are more difficult to filter for the CLF;
- 4) Ind-couple, which can occur when there is an inductive coupling between the SWIO line and a magnetic field, such as the 13,56 MHz RF field used in contactless applications. Since SWP is always used in conjunction with a contactless interface, special attention has to be paid on this parasitic coupling;
- 5) I<sub>EMI</sub>, which represents any other current noise due to EMIs (Electro-Magnetic Interferences).

So the current seen by the CLF is the sum of all these currents:

$$I_{TOT} = S2 + I_{CAP\text{-}GND} + I_{CAP\text{-}ADJ} + I_{IND\text{-}COUPL} + I_{EMI}$$

The 4 last contributors ( $I_{CAP-GND}$ ,  $I_{CAP-ADJ}$ ,  $I_{IND-COUPL}$  &  $I_{EMI}$ ) have to be minimized such that the CLF only measures S2.

### 4.2 Limiting the noise impacts

Looking at these parasitic contributors in more details, it can be said that:

- To limit the value of Icap-gnd & Icap-add, the values of Cpar-gnd and Cpar-add have to be minimized. This is achieved by limiting the length of the wire (cable) between the CLF and the UICC. It is commonly advised to limit the SWIO track on PCBs to less than 20cm. In a test environment, the cable length should also be limited to a few decimetres.
  - The CLF implements a noise filtering scheme, to remove the current noise present at S1 rise & fall time, but this filtering is limited when the bit period (T) is short: there is not much time to filter current spikes in 590ns, which is the minimum T value specified in ETSI TS 102 613 [i.1]. So, there is a compromise to find between the wire (cable) length and the bit rate used on SWIO: the longer the cable, the lower the bit rate to keep an error-free decoding of S2 in the CLF. In a test environment, it is usually not possible to change the bit rate used by the DUT, so the cable length has to be adapted.
- 2) To limit the impact of I<sub>CAP-ADJ</sub>, it is necessary to keep any adjacent track/cable as far as possible from the SWIO track/cable, assuming that this track/cable carries a dynamic signal with voltage transitions.
- 3) To limit the impact of Ind-coupl, it is necessary to keep any magnetic field away from SWIO, using ferrite to shield SWIO if the field emitter is too close to it.
- 4) To limit the impact of **I**<sub>EMI</sub>, it is necessary to use appropriate shielding, depending on the SWIO line environment.

### 4.3 Derived guidelines to set up a test environment

Consequence for the test environment:

- 1) The length of the cable carrying SWIO between the DUT and the test tool has to be minimized (a few decimetres).
- 2) This cable has to be kept away from the contactless RF Field (13,56 MHz).
- 3) This cable also has to be kept away from the cable connecting the contactless antenna.
- 4) In this cable, the SWIO line has to be smelded from the other carried signals (CLK, I/O, RESET).

These guidelines are summarized in figure 4.2 and 4.3.