
IEC 60822 VSB – Vzporedni podsistem vodila IEC 60821 VMEbus

IEC 60822 VSB - Parallel sub-system Bus of the IEC 60821 VMEbus

IEC 60822 VSB - Parallel-Unterbussystem für den IEC 60821 VME-Bus

CEI 60822 VSB - Bus parallèle de sous-système de bus CEI 60821 VME bus

Ta slovenski standard je istoveten z: HD 576 S1:1990[SIST HD 576 S1:1997](https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997)<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>**ICS:**

35.160 Mikroprocesorski sistemi Microprocessor systems

SIST HD 576 S1:1997**en**

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST HD 576 S1:1997](#)

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>

CENELEC

Rue de Stassart, 35 - 1050 Bruxelles
 Tél.: (+ 32 2) 519.68.71 - Fax: (+ 32 2) 519.69.19
 Teletex 206 2210097 - CENEL - Tx 172210097

HD 576 S1

October 1990

ENGLISH VERSION

UDC: 681.3.01:621.3.037

Descriptors: VSB bus

IEC 822 VSB
 PARALLEL SUB-SYSTEM BUS OF THE IEC 821 VME Bus

CEI 822 VSB
 Bus parallèle de sous-système
 du bus CEI 821 VME bus

IEC 822 VSB
 Parallel-Unterbussystem
 für den IEC 821 VME-Bus

BODY OF THE HD

The Harmonization Document consists of:

- IEC 822:1988; IEC/SC 47B, not appended

This Harmonization Document was approved by CENELEC on 1990-06-01.

The English and French versions of this Harmonization Document are provided by the text of the IEC publication and the German version is the official translation of the IEC text.

According to the CENELEC Internal Regulations the CENELEC member National Committees are bound:

to announce the existence of this Harmonization Document at national level by or before 1990-12-15

to publish their new harmonized national standard by or before 1991-06-15

to withdraw all conflicting national standards by or before 1991-06-15.

Harmonized national standards are listed on the HD information sheet, which is available from the CENELEC National Committees or from the CENELEC Central Secretariat.

SIST HD 576 S1:1997

The CENELEC National Committees are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

© Copyright reserved to all CENELEC members

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST HD 576 S1:1997](#)

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>

NORME
INTERNATIONALE
INTERNATIONAL
STANDARD

CEI
IEC

60822

Première édition
First edition
1988-12

CEI 822 VSB

Bus parallèle de sous-système
du bus CEI 821 VMEbus

iTeh STANDARD PREVIEW

(standards.iteh.ai)

IEC 822 VSB

Parallel Sub-system Bus of the
IEC 821 VMEbus

© IEC 1988 Droits de reproduction réservés — Copyright - all rights reserved

Aucune partie de cette publication ne peut être reproduite ni utilisée sous quelque forme que ce soit et par aucun procédé, électronique ou mécanique, y compris la photocopie et les microfilms, sans l'accord écrit de l'éditeur.

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Electrotechnical Commission
Telefax: +41 22 919 0300

3, rue de Varembé Geneva, Switzerland
e-mail: inmail@iec.ch IEC web site <http://www.iec.ch>



Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE XG

Pour prix, voir catalogue en vigueur
For price, see current catalogue

CONTENTS

	Page
FOREWORD	15
PREFACE	15

CHAPTER 0: SCOPE

CHAPTER 1: INTRODUCTION TO THE IEC 822 VSB BUS STANDARD

Section

1.1	Standard objectives of the IEC 822 VSB parallel Subsystem Bus of the IEC 821 VMEbus (Subsystem henceforth referred to as VSB)	19
1.2	VSB system elements	19
1.2.1	Basic definitions	19
1.2.1.1	Physical structure definition	19
1.2.1.2	Functional structure definition	21
1.2.1.3	Types of VSB cycles	25
1.3	VSB standard diagrams	31
1.4	Standard terminology	31
1.4.1	Signal line states	33
1.4.2	Use of the asterisk (*)	35
1.5	Protocol specification	35

SIST HD 576 S1:1997

[https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-](https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-8673dec984/sist-hd-576-s1-1997)

CHAPTER 2: VSB DATA TRANSFER BUS

2.1	Introduction	39
2.2	Data Transfer Bus lines	41
2.2.1	Addressing lines	41
2.2.1.1	AD00-AD31	41
2.2.1.2	SPACE0-SPACE1	43
2.2.1.3	SIZE0-SIZE1	43
2.2.1.4	ASACK0*-ASACK1*	43
2.2.1.5	GA0-GA2	45
2.2.2	Data lines AD00-AD31	45
2.2.3	Control lines	45
2.2.3.1	PAS*	45
2.2.3.2	AC	47
2.2.3.3	WR*	47
2.2.3.4	LOCK*	47
2.2.3.5	DS*	47
2.2.3.6	WAIT*	47
2.2.3.7	ACK*	49
2.2.3.8	ERR*	49
2.2.3.9	IRQ*	49
2.2.3.10	CACHE*	51
2.3	DTB modules - Basic description	51
2.3.1	MASTER	53
2.3.2	SLAVE	55

Section	Page
2.4 Capabilities of MASTERS and SLAVES	57
2.4.1 Addressing capabilities	61
2.4.1.1 Basic addressing capabilities	63
2.4.1.2 ADDRESS-ONLY capability	65
2.4.2 Data transfer capabilities	67
2.4.2.1 Basic data transfer capability of MASTERS	67
2.4.2.2 Basic data transfer capabilities of SLAVES	69
2.4.2.3 Dynamic bus sizing	71
2.4.2.4 SINGLE-TRANSFER capability	73
2.4.2.5 BLOCK-TRANSFER capability	75
2.4.2.6 INDIVISIBLE-ACCESS capability	79
2.4.3 Interrupt capability	83
2.4.3.1 Basic interrupt capabilities of MASTERS and SLAVES	83
2.4.3.2 INTERRUPT-ACKNOWLEDGE cycle capabilities	87
2.5 Interaction between MASTERS and SLAVES	91
2.5.1 Interaction between MASTERS and SLAVES during address broadcast phase	93
2.5.1.1 Flow of the address broadcast phase	93
2.5.1.2 Signaling during the address broadcast phase	99
2.5.2 Interaction between MASTERS and SLAVES during the data transfer	105
2.5.2.1 Flow of a write data transfer	107
2.5.2.2 Flow of a read data transfer	113
2.5.2.3 Signaling during the data transfer phase	117
2.5.3 Interaction between MASTERS and SLAVES during cycle termination	125
2.5.3.1 Flow of the termination of a cycle	125
2.5.4 Interaction between the IHV MASTER and SLAVES during the INTERRUPT-ACKNOWLEDGE cycles	127
2.5.4.1 Flow of an INTERRUPT-ACKNOWLEDGE cycle	129
2.5.4.2 Signaling during the INTERRUPT-ACKNOWLEDGE cycle	137
2.6 Data transfer bus timing specifications	139

CHAPTER 3: VSB DATA TRANSFER BUS ARBITRATION

3.1 Introduction	189
3.1.1 Types of Arbitration	191
3.2 Arbitration Bus lines	191
3.2.1 BREQ*	191
3.2.2 BUSY*	191
3.2.3 BGIN*/BGOUT*	193
3.3 Arbitration modules - Basic description	193
3.3.1 ARBITER	193
3.3.2 REQUESTER	195
3.4 Capabilities of the REQUESTER	199
3.4.1 Serial Arbitration	201
3.4.1.1 Interaction between the ARBITER and SER REQUESTERS	203
3.4.1.2 Signaling during Serial Arbitration	209

Section	Page	
3.4.2	Parallel Arbitration capability	213
3.4.2.1	Flow of an ARBITRATION cycle	213
3.4.2.2	Signaling during the ARBITRATION cycle	219
3.4.3	Power-up sequence	221
3.4.3.1	Flow of the power-up sequence	221
3.4.3.2	Interaction between arbitration bus modules during power-up ..	227
3.5	Interaction between the MASTER, its associated REQUESTER and/or its associated ARBITER	229
3.5.1	Acquisition of the DTB	229
3.5.2	Release of the DTB	229
3.5.3	Race conditions between MASTER requests and ARBITER grants ..	231
3.6	Arbitration bus timing specifications.....	231

CHAPTER 4: ELECTRICAL CHARACTERISTICS OF VSB BOARDS

4.1	Introduction	253
4.1.1	Terminology	253
4.2	Power distribution	257
4.2.1	D.C. voltage characteristics	257
4.2.2	Connector electrical ratings	257
4.3	Bus driving and receiving requirements	257
4.3.1	General	257
4.3.2	Driving and loading RULES for three-state lines (AD00-AD31, DS*, PAS*, LOCK*, SIZE0-SIZE1, SPACE0-SPACE1, WR*)	261
4.3.3	Driving and loading RULES for open-collector lines (AC, ACK*, AD24-AD31, ASACK0*-ASACK1*, BREQ*, BUSY*, CACHE*, ERR*, IRQ*, WAIT*)	265
4.3.4	Driving and loading RULES for BGIN* and BGOUT*	269
4.3.5	Receiving RULES for the geographical addressing lines (GA0-GA2)	271
4.3.6	Additional information	271
4.4	Signal lines interconnection - Summary	273

CHAPTER 5: VSB BACKPLANE SPECIFICATIONS

5.1	Introduction	277
5.2	Backplane physical characteristics	277
5.3	Power distribution	281
5.4	Backplane electrical characteristics	281
5.4.1	Characteristic impedance	281
5.4.2	Termination networks	289
5.5	Signal line interconnection	293
5.5.1	General	293
5.5.2	BGIN*/BGOUT* daisy-chain	295
5.5.3	Geographical addressing	295
5.5.4	Additional information	297
5.6	VSB pin assignment	297
APPENDIX A	301

Figure	Page
1-1 Functional modules and sub-buses defined by the VSB standard ...	23
1-2 Signal timing notation	37
2-1 Data Transfer Bus functional block diagram	39
2-2 Block diagram: MASTER	53
2-3 Block diagram: SLAVE	55
2-4 General flow of a VSB cycle	59
2-5 General flow of an ADDRESS-ONLY cycle	65
2-6 Organization of data	67
2-7 General flow of a SINGLE-TRANSFER cycle	73
2-8 General flow of a BLOCK-TRANSFER cycle	77
2-9 General flow of an INTERRUPT-ACKNOWLEDGE cycle	87
2-10 Flow of the address broadcast phase	97
2-11 Flow of a write data transfer	111
2-12 Flow of a read data transfer	115
2-13 Flow of the termination of the cycle	127
2-14 Flow of an INTERRUPT-ACKNOWLEDGE cycle	133
2-15 Active MASTER, active IHV MASTER and active PAR REQUESTER, LOCK*, WR*, SIZE0-SIZE1 and SPACE0-SPACE1 timing, SINGLE-TRANSFER, BLOCK-TRANSFER, INTERRUPT-ACKNOWLEDGE and ARBITRATION cycles	147
2-16 Active MASTER and SLAVES, address broadcast timing, ADDRESS-ONLY, SINGLE-TRANSFER and BLOCK-TRANSFER cycles	149
2-17 Active MASTER and SLAVES, cycle termination ADDRESS-ONLY cycles	151
2-18 Active MASTER and SLAVES, write data transfer timing, SINGLE-TRANSFER and BLOCK-TRANSFER cycles	153
2-19 Active MASTER and SLAVES, read data transfer timing, SINGLE-TRANSFER, BLOCK-TRANSFER and INTERRUPT-ACKNOWLEDGE cycles	157
2-20 IHV MASTER and INTV SLAVES, selection phase INTERRUPT- ACKNOWLEDGE cycles	161
2-21 MASTERS and SLAVES intercycle timing	163
2-22 DTB control transfer timing	165
2-23 Skew between ASACK0* and ASACK1*	167
2-24 Skew between ACK* and ERR*	167
3-1 Arbitration bus functional block diagram	189
3-2 Block diagram: ARBITER	195
3-3 Block diagram: SER REQUESTER	197
3-4 Block diagram: PAR REQUESTER	199
3-5 Serial Arbitration flow diagram: two REQUESTERS	205
3-6 General flow of an ARBITRATION cycle	213
3-7 Flow of an ARBITRATION cycle	217
3-8 Flow of the power-up sequence	225
3-9 Active PAR REQUESTER, contending PAR REQUESTER and idle SLAVE ARBITRATION cycle	237
3-10 Power-up timing	239

Figure	Page
4-1 VSB signal levels	259
5-1 VSB backplane dimensions	279
5-2 Cross-section of a backplane microstrip signal line	283
5-3 Z_0 versus line width	285
5-4 C_0 versus line width	285
5-5 Standard bus termination	291
5-6 BGIN*/BGOUT* daisy-chain illustration	295
5-7 Geographical addressing lines resistor/capacitor circuit	295
A1 Flow of the selection phase	303
A2 Selection phase control; a high level block diagram	305
A3 An example for the selection logic	307

Table

2-1 RULES and PERMISSIONS that specify the use of the dotted lines by the various types of MASTERS	53
2-2 RULES and PERMISSIONS that specify the use of the dotted lines by the various types of SLAVES	55
2-3 Mnemonics that specify addressing capabilities	63
2-4 Mnemonic that specifies ADDRESS-ONLY capability	65
2-5 Mnemonics that specify the basic data transfer capabilities of SLAVES	69
2-6 Mnemonic that specifies BLOCK-TRANSFER capability	79
2-7 Mnemonics that specify interrupt capabilities	85
2-8 Mnemonics that specify STATUS/ID transfer capabilities of IHV MASTERS and INTV SLAVES	91
2-9 Use of SPACE0 and SPACE1 to select the address space	99
2-10 Encoding of SIZE0 and SIZE1 for requested size of the transfer ..	101
2-11 Use of AD00 and AD01 to select the lowest addressed byte location to be accessed	101
2-12 Encoding of SIZE0, SIZE1, AD00 and AD01 to define the byte locations to be accessed	103
2-13 Encoding of ASACK0* and ASACK1* to define the size of the SLAVE	105
2-14 Placement of valid data on AD00-AD31 by the active MASTER during write cycles	117
2-15 Use of AD00-AD31 by a D32 SLAVE to access byte locations	119
2-16 Use of AD16-AD31 by a D16 SLAVE to access byte locations	121
2-17 Use of AD24-AD31 by a D08 SLAVE to access byte locations	121
2-18 Use of SPACE0, SPACE1 and WR* to select an INTERRUPT-ACKNOWLEDGE cycle	137
2-19 Use of the data lines by D08, D16 and D32 INTV SLAVES during INTERRUPT-ACKNOWLEDGE cycles	139
2-20 Active MASTER, responding SLAVE, participating SLAVE and idle SLAVE timing parameters	143
2-21 IHV MASTER, responding INTV SLAVE, contending INTV SLAVE and idle SLAVE timing parameters	145
2-22 MASTER, timing specifications	169
2-23 SLAVE, timing specifications	179

Table	Page
3-1 RULES and PERMISSIONS that specify the use of the dotted lines by the various types of SER REQUESTERS	197
3-2 Mnemonics that are used to describe REQUESTERS	201
3-3 Use of SPACE0-SPACE1 and WR* to select an ARBITRATION cycle	219
3-4 Active PAR REQUESTER, contending PAR REQUESTER and idle SLAVE timing parameters	233
3-5 Power-up timing parameters	235
3-6 Active REQUESTER timing specifications	241
3-7 Contending REQUESTER timing specifications	245
3-8 Power-up timing specifications	249
4-1 Bus driving and receiving requirements	261
4-2 Signal line interconnection - Summary	275
5-1 Bus voltage specification	281
5-2 Signal line termination	293
5-3 Geographical addressing slot assignment	297
5-4 VSB pin assignment	299

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST HD 576 S1:1997

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>

INTERNATIONAL ELECTROTECHNICAL COMMISSION

IEC 822 VSB

PARALLEL SUB-SYSTEM BUS
OF THE IEC 821 VMEbus

FOREWORD

- 1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.
- 2) They have the form of recommendations for international use and they are accepted by the National Committees in that sense.
- 3) In order to promote international unification, the IEC expresses the wish that all National Committees should adopt the text of the IEC recommendation for their national rules in so far as national conditions will permit. Any divergence between the IEC recommendation and the corresponding national rules should, as far as possible, be clearly indicated in the latter.
- 4) The IEC has not laid down any procedure concerning marking as an indication of approval and has no responsibility when an item of equipment is declared to comply with one of its recommendations.

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecf8a4/sist-hd-576-s1-1997>

PREFACE

This standard has been prepared by Sub-Committee 47B: Microprocessor Systems, of IEC Technical Committee No. 47: Semiconductor Devices.

The text of this standard is based on the following documents:

Six Months' Rule	Report on Voting
47B(C0)22	47B(C0)27

Further information can be found in the Report on Voting indicated in the table above.

The following IEC publications are quoted in this standard:

Publications Nos. 603-2 (1980): Connectors for frequencies below 3 MHz for use with printed boards, Part 2: Two-part connectors for printed boards, for basic grid of 2.54 mm (0.1 in) with common mounting features.

821 (1987): IEC 821 BUS - Microprocessor system bus for 1 to 4 byte data.

IEC 822 VSB
PARALLEL SUB-SYSTEM BUS
OF THE IEC 821 VMEbus

CHAPTER 0: SCOPE

The introduction of high performance of 32-bit microprocessors, as well as the demands placed on microcomputers by the user community have created a need for multiprocessor systems built from board level products. The increase in the number of functions that such systems provided necessitated the introduction of a sophisticated subsystem bus. The VSB (VME Subsystem Bus) was designed to respond to these requirements.

It includes a high speed asynchronous data transfer bus which allows masters to direct the transfer of binary data to and from slaves. The master initiates bus cycles in order to transfer data between itself and slaves. The slave detects bus cycles that are initiated by the active master and, when those cycles select it, transfers data between itself and the master.

(standards.iteh.ai)

Four types of cycles are defined: an address-only cycle, a single transfer cycle, a block transfer cycle, and an interrupt acknowledge cycle. To maximize data transfer rates in multiprocessor systems, the VSB standard defines a mechanism that allows the master to broadcast the data to any number of slaves in the course of a single cycle. In addition, the data transfer mechanism supports dynamic bus sizing as well as resource locking and data caching.

The arbitration bus is the second of the two sub-buses defined in the VSB standard. It allows arbiter modules and/or requester modules to coordinate the use of the data transfer bus. Two arbitration methods are defined - a serial arbitration method and a parallel (distributed) arbitration method. These arbitration methods provide protocols to implement an array of subsystem architectures. Using the serial arbitration method, a designer can implement a single master subsystem that includes a single processor board requiring access to large amounts of memory. This method could be used to build a system that gives priority to a primary master that, when it can, grants the bus to other secondary masters. At the other end of the spectrum, a multiprocessing subsystem can be implemented using the parallel arbitration method.

CHAPTER 1: INTRODUCTION TO THE IEC 822 VSB BUS STANDARD

1.1 *Standard objectives of the IEC 822 VSB parallel Subsystem Bus of the IEC 821 VMEbus (Subsystem henceforth referred to as VSB)*

This VSB bus is a local subsystem extension bus. It allows a processor board to access additional memory and I/O over a local bus, removing traffic from the global bus and improving the total throughput of the system. The system has been conceived with the following objectives:

- a) To improve the performance of multiprocessor systems by allowing the design of local subsystems.
- b) To specify the electrical characteristics required to design boards that will reliably transfer data over the VSB.
- c) To specify the mechanical requirements to be compatible with VSB systems.
- d) To specify protocols that precisely define the interaction between the VSB and devices interfaced to it.
- e) To provide terminology and definitions that describe VSB protocols.

ITeH STANDARD PREVIEW
(standards.iteh.ai)

1.2 *VSB system elements*

SIST HD 576 S1:1997

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>

1.2.1 *Basic definitions*

The structure of the VSB can be described from two points of view: its mechanical structure and its functional structure.

Because the primary use of the VSB is as a secondary bus, there are no mechanical specifications of VSB board level, and/or box level products. It is assumed that products that include the VSB have been designed to comply with the mechanical specifications of the global system bus. Therefore, the VSB standard only describes the physical dimensions of the backplane.

The functional specifications of the VSB describe how the bus works, what functional modules participate in its various operations, and the rules that govern their behavior. This paragraph provides informal definitions for the basic terms used to describe both the mechanical and functional structure of the VSB.

1.2.1.1 *Physical structure definition*

BOARD

A printed circuit (PC) board, its collection of electronic components, and at least one 96-pin connector.

VSB BACKPLANE

An assembly that includes a printed circuit (PC) board and 96-pin connectors. The backplane buses the 64 pins on the two outer rows of the VSB connectors, providing the signal paths needed for VSB operation.

SLOT

A position where a board can be inserted into a backplane. Each VSB slot provides at least one 96-pin connector.

SUBRACK

A rigid framework that provides mechanical support for boards inserted into the backplane, ensuring that the connectors mate properly and that adjacent boards do not contact each other. It also guides the cooling airflow through the system, and ensures that inserted boards are not disengaged from the backplane due to vibration.

1.2.1.2 Functional structure definition

Figure 1-1, page 23, shows a block diagram of the functional modules and sub-buses defined by the VSB standard.

BACKPLANE INTERFACE LOGIC

Special interface logic that takes into account the characteristics of the backplane. The VSB standard prescribes certain requirements for the design of this logic, which take into account the signal line impedance, propagation times, termination values, the maximum length of the backplane and the number of slots allowed.

<https://standards.iteh.ai/catalog/standards/sist/b6117646-f8d2-4460-9507-867ddecff8a4/sist-hd-576-s1-1997>

FUNCTIONAL MODULE

A collection of electronic circuitry that resides on one board and works to accomplish a specific task. Functional modules are used as a vehicle for discussing bus protocols, and should not be considered to constrain the design of actual logic.

DATA TRANSFER BUS

One of the two sub-buses defined in the VSB standard. It allows MASTERS to direct the transfer of binary data to and from SLAVES. (The VSB Data Transfer Bus is often abbreviated DTB.) The DTB contains 32 multiplexed address/data lines and the associated control signals that are required to execute cycles on the VSB.

MASTER

A functional module that initiates bus cycles in order to transfer data between itself and VSB SLAVES. The MASTER that is currently in control of the DTB is referred to as the active MASTER.

SLAVE

A functional module that detects bus cycles initiated by the active MASTER and, when those cycles select it, transfers data between itself and the MASTER. The VSB standard defines a mechanism through which any number of SLAVES can participate in a bus cycle.