SLOVENSKI STANDARD
SIST HD 576 S1:1997

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IEC 60822 VSB – Vzporedni podsistem vodila IEC 60821 VMEbus

IEC 60822 VSB - Parallel sub-system Bus of the IEC 60821 VMEbus

IEC 60822 VSB - Parallel-Unterbussystem für den IEC 60821 VME-Bus

CEI 60822 VSB - Bus parallèle de sous-système de bus CEI 60821 VME bus

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PARALLEL SUB-SYSTEM BUS OF THE IEC 821 VME Bus

CEI 822 VSB
Bus parallèle de sous-système
du bus CEI 821 VME bus

IEC 822 VSB
Parallel-Unterbussystem
für den IEC 821 VME-Bus

BODY OF THE HD

The Harmonization Document consists of:

- IEC 822:1988; IEC/SC 47B, not appended

This Harmonization Document was approved by CENELEC on 1990-06-01.

The English and French versions of this Harmonization Document are provided by the text of the IEC publication and the German version is the official translation of the IEC text.

According to the CENELEC Internal Regulations the CENELEC member National Committees are bound:

to announce the existence of this Harmonization Document at national level by or before 1990-12-15

to publish their new harmonized national standard by or before 1991-06-15

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NORME INTERNATIONALE

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Bus parallèle de sous-système du bus CEI 821 VMEbus

IEC 822 VSB

Parallel Sub-system Bus of the IEC 821 VMEbus

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

IEC 822 VSB

PARALLEL SUB-SYSTEM BUS OF THE IEC 821 VMEbus

FOREWORD

1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.

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4) The IEC has not laid down any procedure concerning marking as an indication of approval and has no responsibility when an item of equipment is declared to comply with one of its recommendations.

PREFACE

This standard has been prepared by Sub-Committee 47B: Microprocessor Systems, of IEC Technical Committee No. 47: Semiconductor Devices.

The text of this standard is based on the following documents:

Six Months' Rule	Report on Voting
47B(CO)22	47B(CO)27

Further information can be found in the Report on Voting indicated in the table above.

The following IEC publications are quoted in this standard:

Publications Nos. 603-2 (1980): Connectors for frequencies below 3 MHz for use with printed boards, Part 2: Two-part connectors for printed boards, for basic grid of 2.54 mm (0.1 in) with common mounting features.

821 (1987): IEC 821 BUS - Microprocessor system bus for 1 to 4 byte data.

IEC 822 VSB

PARALLEL SUB-SYSTEM BUS OF THE IEC 821 VMEbus

CHAPTER 0: SCOPE

The introduction of high performance of 32-bit microprocessors, as well as the demands placed on microcomputers by the user community have created a need for multiprocessor systems built from board level products. The increase in the number of functions that such systems provided necessitated the introduction of a sophisticated subsystem bus. The VSB (VME Subsystem Bus) was designed to respond to these requirements.

It includes a high speed asynchronous data transfer bus which allows masters to direct the transfer of binary data to and from slaves. The master initiates bus cycles in order to transfer data between itself and slaves. The slave detects bus cycles that are initiated by the active master and, when those cycles select it, transfers data between itself and the master.

Four types of cycles are defined: an address-only cycle, a single transfer cycle, a block transfer cycle, and an interrupt acknowledge cycle. To maximize data transfer rates in multiprocessor systems, the VSB standard defines a mechanism that allows the master to broadcast the data to any number of slaves in the course of a single cycle. In addition, the data transfer mechanism supports dynamic bus sizing as well as resource locking and data caching.

The arbitration bus is the second of the two sub-buses defined in the VSB standard. It allows arbiter modules and/or requester modules to coordinate the use of the data transfer bus. Two arbitration methods are defined - a serial arbitration method and a parallel (distributed) arbitration method. These arbitration methods provide protocols to implement an array of subsystem architectures. Using the serial arbitration method, a designer can implement a single master subsystem that includes a single processor board requiring access to large amounts of memory. This method could be used to build a system that gives priority to a primary master that, when it can, grants the bus to other secondary masters. At the other end of the spectrum, a multiprocessing subsystem can be implemented using the parallel arbitration method.

CHAPTER 1: INTRODUCTION TO THE IEC 822 VSB BUS STANDARD

1.1 *Standard objectives of the IEC 822 VSB parallel Subsystem Bus of the IEC 821 VMEbus (Subsystem henceforth referred to as VSB)*

This VSB bus is a local subsystem extension bus. It allows a processor board to access additional memory and I/O over a local bus, removing traffic from the global bus and improving the total throughput of the system. The system has been conceived with the following objectives:

a) To improve the performance of multiprocessor systems by allowing the design of local subsystems.

b) To specify the electrical characteristics required to design boards that will reliably transfer data over the VSB.

c) To specify the mechanical requirements to be compatible with VSB systems.

d) To specify protocols that precisely define the interaction between the VSB and devices interfaced to it.

e) To provide terminology and definitions that describe VSB protocols.

1.2 *VSB system elements*

1.2.1 *Basic definitions*

The structure of the VSB can be described from two points of view: its mechanical structure and its functional structure.

Because the primary use of the VSB is as a secondary bus, there are no mechanical specifications of VSB board level, and/or box level products. It is assumed that products that include the VSB have been designed to comply with the mechanical specifications of the global system bus. Therefore, the VSB standard only describes the physical dimensions of the backplane.

The functional specifications of the VSB describe how the bus works, what functional modules participate in its various operations, and the rules that govern their behavior. This paragraph provides informal definitions for the basic terms used to describe both the mechanical and functional structure of the VSB.

1.2.1.1 *Physical structure definition*

BOARD

A printed circuit (PC) board, its collection of electronic components, and at least one 96-pin connector.

VSB BACKPLANE
An assembly that includes a printed circuit (PC) board and 96-pin connectors. The backplane buses the 64 pins on the two outer rows of the VSB connectors, providing the signal paths needed for VSB operation.

SLOT
A position where a board can be inserted into a backplane. Each VSB slot provides at least one 96-pin connector.

SUBRACK
A rigid framework that provides mechanical support for boards inserted into the backplane, ensuring that the connectors mate properly and that adjacent boards do not contact each other. It also guides the cooling airflow through the system, and ensures that inserted boards are not disengaged from the backplane due to vibration.

1.2.1.2 *Functional structure definition*

Figure 1-1, page 23, shows a block diagram of the functional modules and sub-buses defined by the VSB standard.

BACKPLANE INTERFACE LOGIC
Special interface logic that takes into account the characteristics of the backplane. The VSB standard prescribes certain requirements for the design of this logic, which take into account the signal line impedance, propagation times, termination values, the maximum length of the backplane and the number of slots allowed.

FUNCTIONAL MODULE
A collection of electronic circuitry that resides on one board and works to accomplish a specific task. Functional modules are used as a vehicle for discussing bus protocols, and should not be considered to constrain the design of actual logic.

DATA TRANSFER BUS
One of the two sub-buses defined in the VSB standard. It allows MASTERS to direct the transfer of binary data to and from SLAVES. (The VSB Data Transfer Bus is often abbreviated DTB.) The DTB contains 32 multiplexed address/data lines and the associated control signals that are required to execute cycles on the VSB.

MASTER
A functional module that initiates bus cycles in order to transfer data between itself and VSB SLAVES. The MASTER that is currently in control of the DTB is referred to as the active MASTER.

SLAVE
A functional module that detects bus cycles initiated by the active MASTER and, when those cycles select it, transfers data between itself and the MASTER. The VSB standard defines a mechanism through which any number of SLAVES can participate in a bus cycle.