SLOVENSKI STANDARD
SIST HD 593.1 S1:1997

01-avgust-1997

Mikroprocesorski sistem BUS za 8- in 16-bitne podatke (MULTIBUS I) - 1. del: Funkcionalni opis z električnimi in časovnimi specifikacijami (IEC 60796-1:1990)

Microprocessor system BUS - 8-bit and 16-bit data (MULTIBUS I) -- Part 1: Functional description with electrical and timing specifications

Mikroprozessor-Systembus I für 8 Bit- und 16 Bit-Datenübertragung (MULTIBUS I) -- Teil 1: Funktionsbeschreibung, elektrische Anforderungen und Zeitverhalten

BUS système à microprocesseurs - Données: 8 bits et 16 bits (MULTIBUS 1) -- Partie 1: Description fonctionnelle avec spécifications électriques et chronologiques

Ta slovenski standard je istoveten z: **HD 593.1 S1:1992**

ICS:

35.160	Mikroprocesorski sistemi	Microprocessor systems

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HARMONIZATION DOCUMENT

DOCUMENT D'HARMONISATION

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HD 593.1 S1

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ENGLISH VERSION

Microprocessor system bus - 8-bit and 16-bit data (MULTIBUS I)
Part 1: Functional description with electrical and timing specifications
(IEC 796-1:1990)

Bus système à microprocesseurs Données: 8 bits et 16 bits (MULTIBUS I)
Première partie: Description fonctionnelle avec spécifications électriques et chronologiques
(CEI 796-1:1990)

Mikroprozessor-Systembus I für 8 Bit- und 16 Bit-Datenübertragung (MULTIBUS I)
Teil 1: Funktionsbeschreibung, elektrische Anforderungen und Zeitverhalten

(IEC 796-1:1990)

This Harmonization Document was approved by CENELEC on 1992-06-16. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for implementation of this Harmonization Document on a national level.

Up-to-date lists and bibliographical references concerning national implementation may be obtained on application to the Central Secretariat or to any CENELEC member.

This Harmonization Document exists in three official versions (English, French, German).

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

Ref. No. HD 593.1 S1:1992 E

FOREWORD

The CENELEC questionnaire procedure, performed for finding out whether or not the International Standard IEC 796-1:1990 could be accepted without textual changes, has shown that no common modifications were necessary for the acceptance as Harmonization Document.

The reference document was submitted to the CENELEC members for formal vote and was approved by CENELEC as HD 593.1 S1 on 16 June 1992.

The following dates were fixed:

- latest date of announcement of the HD at national level	(doa)	1992-12-01
- latest date of publication of a harmonized national standard	(dop)	1993-06-01
- latest date of withdrawal of conflicting national standards	(dow)	1993-06-01

For products which have complied with the relevant national standard before 1993-06-01, as shown by the manufacturer or by a certification body, this previous standard may continue to apply for production until 1998-06-01.

Annexes designated "normative" are part of the body of the standard. In this standard, annex ZA is normative.

ENDORSEMENT NOTICE

The text of the International Standard IEC 796-1:1990 was approved by CENELEC as a Harmonization Document without any modification.

ANNEX ZA (normative)

OTHER INTERNATIONAL PUBLICATIONS QUOTED IN THIS STANDARD WITH THE REFERENCES OF THE RELEVANT EUROPEAN PUBLICATIONS

When the international publication has been modified by CENELEC common modifications, indicated by (mod), the relevant EN/HD applies.

IEC Publication	Date	Title	EN/HD	Date
625-1	1979	An interface system for programmable measuring instruments (byte serial, bit parallel) - Part 1: Functional specifications, electrical specifications, mechanical specifications, system applications and requirements for the designer and user	HD 414.1 S1	1981

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Bus système à microprocesseurs – Données: 8 bits et 16 bits (MULTIBUS I)

Première partie:
Description fonctionnelle avec spécifications électriques et chronologiques

Microprocessor system bus – 8-bit and 16-bit data (MULTIBUS I)

Part 1:
Functional description with electrical and timing specifications

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MICROPROCESSOR SYSTEM BUS - 8-BIT AND 16-BIT DATA (MULTIBUS I)

Part 1: Functional description with electrical and timing specifications

FOREWORD

1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.

2) They have the form of recommendations for international use and they are accepted by the National Committees in that sense.

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4) The IEC has not laid down any procedure concerning marking as an indication of approval and has no responsibility when an item of equipment is declared to comply with one of its recommendations.

PREFACE

This standard has been prepared by Sub-Committee 47B*: Microprocessor Systems, of IEC Technical Committee No. 47: Semiconductor Devices.

This standard forms Part 1 of a series of publications, the other parts being:

- Publication 796-2 (1990): Microprocessor system bus - 8-bit and 16-bit data (MULTIBUS I) - Part 2: Mechanical and pin descriptions for the system bus configuration, with edge connectors (direct).

- Publication 796-3 (1990): Part 3: Mechanical and pin descriptions for the Eurocard configuration with pin and socket (indirect) connectors.

The text of this standard is based upon the following documents:

Six Months' Rule	Report on Voting
47B(CO)8	47B(CO)14

Full information on the voting for the approval of this standard can be found in the Voting Report indicated in the above table.

The following IEC publication is quoted in this standard:

Publication No. 625-1 (1979): An interface system for programmable measuring instruments (byte serial, bit parallel), Part 1: Functional specifications, electrical specifications, mechanical specifications, system applications and requirements for the designer and user.

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* IEC Sub-Committee 47B has now been transferred to ISO/IEC JTC 1.

This standard was approved according to IEC procedures and is therefore published as an IEC standard.

MICROPROCESSOR SYSTEM BUS - 8-BIT AND 16-BIT DATA (MULTIBUS I)

Part 1: Functional description with electrical and timing specifications

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INTRODUCTION

This standard is one of a series which deals with the electrical and mechanical interfaces to allow various microprocessor system components to interact with each other. The interface bus serves as a parallel transfer and utility signal interconnect for closely coupled system components. The series consists of one functional description and two alternative mechanical standards.

SECTION ONE - GENERAL

1.1 Scope

This standard is applicable to interface system components, for use in interconnecting data processing, data storage, and peripheral control devices in a closely coupled configuration. This interface system contains the necessary signals to allow the various system components to interact with each other. It allows memory and Input/Output (I/O) data transfers, direct memory accesses, generation of interrupts, etc. This standard provides a detailed description of all the elements and features that make up the system bus.

The bus supports two independent address spaces: memory and I/O. During memory cycles the bus allows direct addressability of up to 16 megabytes using 24-bit addressing. During I/O bus cycles, the bus allows addressing of up to 64K I/O ports using 16-bit addressing. Both memory and I/O cycles can support 8-bit data transfers.

The bus structure is built upon the master-slave concept where the master device in the system takes control of the bus and the slave device, upon decoding its address, acts upon the command provided by the master. This handshake (master-slave relationship) between the master and slave devices allows modules of different speeds to be interfaced via the bus. It also allows data rates up to five million transfers per second (bytes or words) to take place across the bus.

Another important feature of the bus is the ability to connect multiple master modules for multiprocessing configurations. The bus provides control signals for connecting multiple masters in either a serial or parallel priority fashion. With either of these two arrangements, more than one master may share bus resources.

This standard has been prepared for those users who intend to evaluate or design products that will be compatible with the system bus structure. To this end, the necessary signal definitions and timing and electrical specifications have been covered in detail.

This standard deals only with the interface characteristics of microcomputer devices and not with design specifications, performance requirements, and safety requirements of modules.

Throughout this standard, the term "system" denotes the byte or word interface system that, in general, includes all the circuits, connectors, and control protocol to effect unambiguous data transfer between devices. The term "device" or "module" denotes any product connected to the interface system that communicates information via the bus, and that conforms to the interface system definition.

1.2 Object

This standard is intended to:

1) define a general purpose microcomputer system bus;

2) specify the device-independent electrical and functional interface requirements that a module shall meet in order to interconnect and communicate unambiguously via the bus system;

3) specify the terminology and definitions related to the system;

4) enable the interconnection of independently manufactured devices into a single functional system;

5) permit products with a wide range of capabilities to be interconnected to the system simultaneously;

6) define a system with a minimum of restrictions on the performance characteristics of devices connected to the system.

1.3 Definitions

The following general definitions apply for the purpose of this standard. More detailed definitions can be found in the relevant sub-clause.

1.3.1 *General System Terms*

1.3.1.1 *Compatibility* (IEC Publication 625-1)

The degree to which devices may be interconnected and used, without modification, when designed as defined throughout this standard (e.g. mechanical, electrical, functional).

1.3.1.2 *Bus Cycle*

The process whereby digital signals effect the transfer of data bytes or words across the interface by means of an interlocked sequence of control signals. "Interlocked" denotes a fixed sequence of events in which one event shall occur before the next event can occur.

1.3.1.3 *Interface* (IEC Publication 625-1)

A common boundary between a considered system and another system, or between parts of a system, through which information is conveyed.

1.3.1.4 *Interface System* (IEC Publication 625-1)

The set of device-independent mechanical, electrical and functional elements of an interface necessary to effect communication among a set of devices. Cables, connectors, driver and receiver circuits, signal line descriptions, timing and control conventions and functional logic circuits are typical system elements.

1.3.1.5 *Override*

A bus master overrides the bus control logic when it is necessary to guarantee itself back-to-back bus cycles. This is called "overriding" or "locking" the bus, temporarily preventing other masters from using the bus.

1.3.1.6 *System*

A set of interconnected elements which achieve a given objective through the performance of a specified function.

1.3.2 *Signals and Paths* (IEC Publication 625-1)

1.3.2.1 *Bus* (IEC Publication 625-1)

A signal line or a set of signal lines used by an interface system to which a number of devices are connected and over which messages are carried.

1.3.2.2 *Byte*

A group of eight concurrent binary digits operated on as a unit.

1.3.2.3 *Word*

Two bytes or sixteen bits operated on as a unit.

1.3.2.4 *Signal* (IEC Publication 625-1)

The physical representation of information.