SLOVENSKI STANDARD

SIST-TP CLC/R217-013:2004

september 2004

Izmenjalni formati - Evalvacija EDIF verzije 3 0 0 nivo 0

Interchange formats - Evaluation of EDIF Version 3 0 0 level 0

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CENELEC

R217-013

REPORT

February 1997

English version

Interchange formats
Evaluation of EDIF Version 3 0 0 level 0

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved by CENELEC on 1996-07-02 and endorsed by the CENELEC Technical Board on 1996-12-09.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Foreword

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Contents

iTeh STANDARD PREVIEW
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SIST-TP CLC/R217-013:2004
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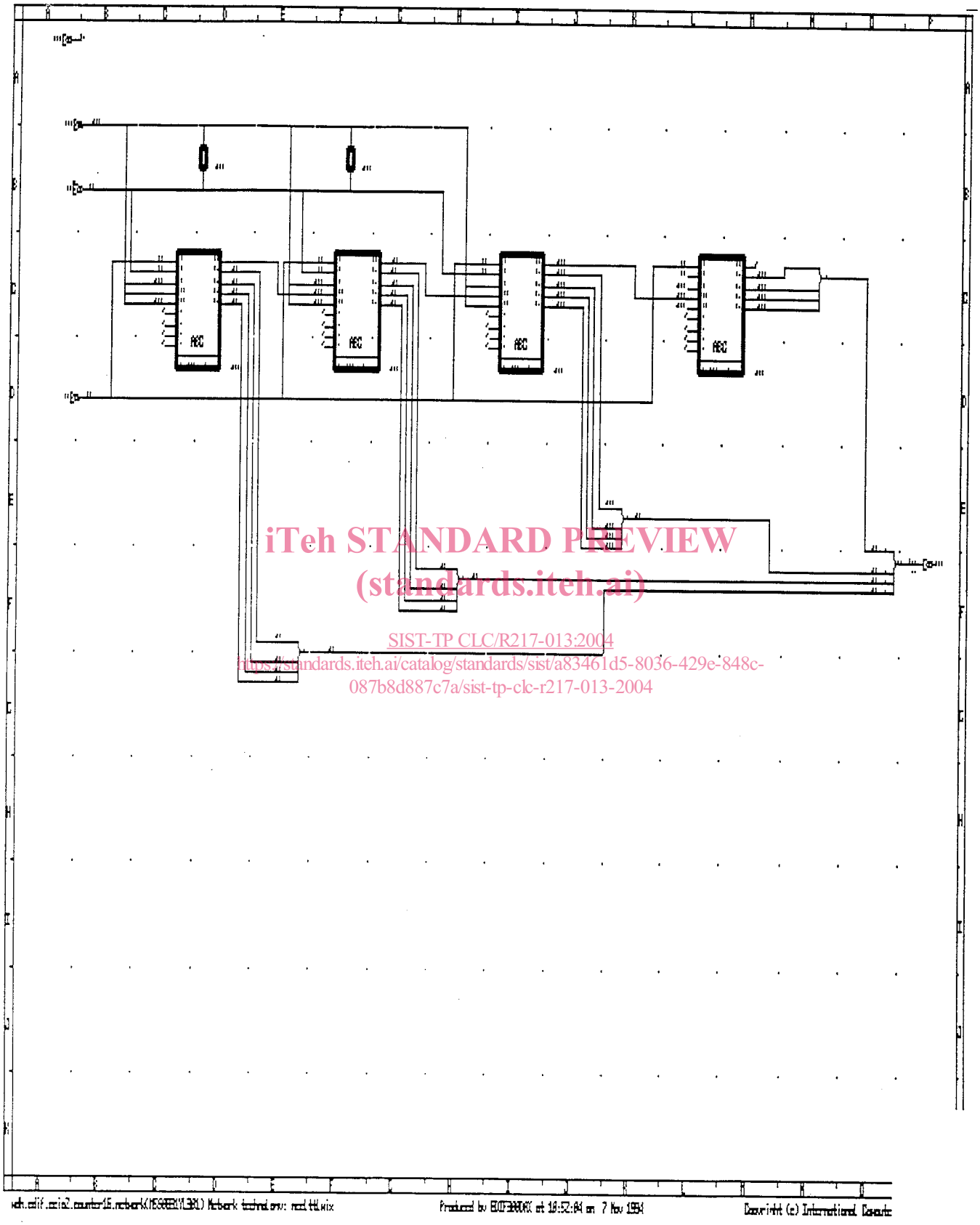

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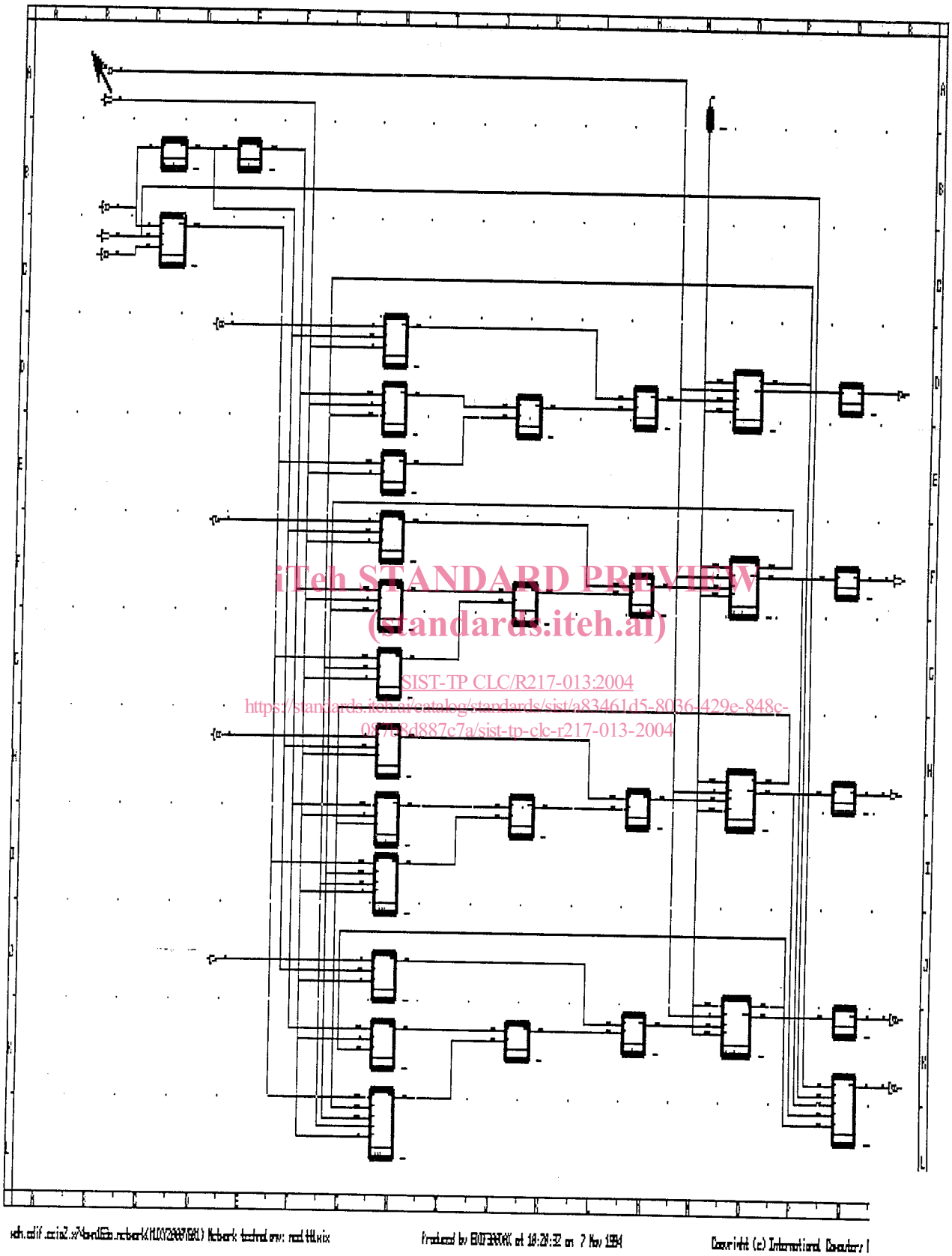
https://standards.iteh.ai/catalog/standards/sist/a83461d5-8036-429e-848c-087b8d887c7a/sist-tp-clc-r217-013-2004



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SIST-TP CLC/R217-013:2004
https://standards.iteh.ai/catalog/standards/sist/a83461d5-8036-429e-848c-08f38d887c7a/sist-tp-clc-r217-013-2004

1 Introduction

There have been major changes to the EDIF concepts between Version 2 0 0 and Version 3 0 0 particularly in the area of schematic transfer. This is the domain in which the majority of current interfaces operate. The deficiencies in Version 2 0 0 have led to difficulties in achieving consistently successful transfer of design data between CAD systems and have brought about numerous unofficial work-arounds which deviate from the standard.

2 Version 2 0 0 versus Version 3 0 0

2.1 Clarified Connectivity Model

2.1.1 Deficiencies in Version 2 0 0:-

a) Nets are in general handled satisfactorily, but the representation of busses is ambiguous and incomplete.
b) The definition and use of rippers is obscure. It is very difficult to determine the implied connectivity
c) View-wide connectivity is not always specified.

2.1.2 Improvements in Version 3 0 0

a) Explicit bus constructs
b) Rippers have been simplified
c) There is now explicit definition of view wide connectivity

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2.2 Improved Schematic Representation

2.2.1 Deficiencies in Version 2 0 0

a) There is no specific support for special diagrammatic representations e.g. OnPageConnectors, Title Blocks, Page Borders
b) There is little support for text representation and grids.
c) Multiple or shared symbols are not supported

2.2.2 Improvements in Version 3 0 0

a) Mechanisms have been provided for the definition of special schematic diagrammatic representations
b) Multiple symbols are now fully supported, there is partial support for shared symbols.
c) There is better support for grids.

2.3 Clearer Model of Design Objects and Instantiation

2.3.1 Deficiencies in Version 2 0 0

a) The semantics of mixed view type instantiation is unclear and very confusing,
b) The view concept and the cell concept are overloaded.

2.3.2 Improvements in Version 3 0 0

a) The instantiation mechanism has been improved
b) The view concept is reserved for design related representations
c) Cell overloading has been removed

2.4 Syntactic Modifications

2.4.1 Changes made in Version 3 0 0:-

a) Symbolic Constants have been removed
b) A more explicit keyword structure has been adopted.
c) Problem areas have been corrected e.g. transformation.
d) Generic constructs such as arrays have been removed and replaced by constructs with improved semantics

2.5 Scope

The scope of version 3 0 0 is more limited than that of Version 2 0 0.

Version 2 0 0 Views	Version 3 0 0 Views
netlist	connectivity
schematic	schematic
masklayout	stub present
PCBlayout	stub present (EDIF4 0 0)
symboliclayout	stub present
logicmodel	stub present
graphic	alternative mechanism
documentation	alternative mechanism
behavior	stub present
stranger	not required

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The above changes are far reaching and present some major changes to the EDIF Interfaces(writers) currently in operation. These changes will be discussed in some detail in the following sections of this document. In the example pieces of EDIF the changes are shown in **bold** type

3 ConnectivityView

3.1 EDIF Header

The addition of an enclosing construct EDIFHeader was all that was required, this involved a trivial change to the code.

3.2 TimeStamp

Again the change here was to enclose the date and time values within their own constructs

3.2.1 EDIF Header Description - Version 2 0 0

```
(EDIF COUNTER
    (EDIFVersion 2 0 0 )
    ( EDIFLevel 0 )
    ( KeywordMap
        ( KeywordLevel 0 ) )
    ( Status
        ( Written
            ( TimeStamp 1993 09 01 13 30 41)
```

(Program "LD2EDIF" (Version "0"))
(Author "W.D.HILCHESON")
(DataOrigin "ICL West Gorton" (Version "1 0"))))

3.2.2 EDIF Header Description - Version 3 0 0

(EDIF COUNTER
(EDIFVersion 3 0 0)
(EDIFHeader
(EDIFLevel 0)
(KeywordMap
(K0KeywordLevel))
(Status
(Written
(TimeStamp (Date 1993 09 01) (Time 16 37 56))
(Program "LD3EDIF" (Version "0"))
(Author "W.D.HILCHESON")
(DataOrigin "ICL West Gorton" (Version "1 0")))))

3.3 Library Header

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Another trivial addition to the code, this is effectively a wrapper for data already defined in Version 2 0 0

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3.3.1 NameCaseSensitivity

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This was implemented as an empty construct in the current implementation of the interfaces. Again it was a trivial change.

3.3.2 UnitDefinitions, ConnectivityUnits

These items required minimal new code to be added to the interface.

3.3.3 SetVoltage & SetCurrent

These items required minimal new code to be added to the interface.

3.3.4. Library Description - Version 2 0 0

(Library NetLibrary
(EDIFLevel 0)
(Technology
(NumberDefinition)
(SimulationInfo
(LogicValue L (Comment "Logic Low"))
(LogicValue H (Comment "Logic High"))
(LogicValue X (Comment "Logic Dont Care"))
(LogicValue Z (Comment "Logic High Impedance"))))
(Status
(Written
(TimeStamp 1993 09 01 13 31 08)
(DataOrigin "ICL West Gorton" (Version "1 0"))))

3.3.5 Library Description - Version 3 0 0

```
(Library NetLibrary
    (LibraryHeader
        (EDIFLevel 0 )
        (NameCaseSensitivity )
        (Technology
            (NumberDefinition
                (UnitDefinitions
                    (Unit nanosecond 1 (E 1 -9) ( Second 1 ))
                    (Unit mV 1 (E 1 -3) ( Volt 1 ))
                    (Unit mA 1 (E 1 -3) ( Ampere 1 )) )
            (ConnectivityUnits
                (SetTime ( UnitRef nanosecond)) ) )
            (SimulationInfo
                (SetVoltage ( UnitRef mV))
                (SetCurrent ( UnitRef mA))
                (LogicValue L ( Comment "Logic Low" ) )
                (LogicValue H ( Comment "Logic High" ) )
                (LogicValue X ( Comment "Logic Don't Care" ) )
                (LogicValue Z ( Comment "Logic High Impedance" ) ) ) )
        (Status
            (Written
                (TimeStamp ( Date 1993 09 01 ) ( Time 16 38 19 ) )
                (DataOrigin "ICL West Gorton" (Version "1 0") ) ) ) ) )
```

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3.4 Clusters

In EDIF Version 3 0 0, views which share a common interface are contained within a cluster. This construct more or less replaces the view construct of Version 2 0 0.

3.4.1 Cell Description - Version 2 0 0

```
( Cell X74F74
    ( CellType GENERIC )
        ( Status
            ( Written
                ( TimeStamp 1993 09 01 13 31 08)
                ( DataOrigin "ICL West Gorton" (Version "M5S083118L00") ) ) )
        ( View NetView
            ( ViewType Netlist )
            ( Interface
                ( Port D ( Direction Input ) )
                ( Port CLK ( Direction Input ) )
                ( Port Pre ( Direction Input ) )
                ( Port Clr ( Direction Input ) )
                ( Port Q ( Direction Output ) )
                ( Port QBar ( Direction Output ) ) ) ) )
```

3.4.2 Cell Description - Version 3 0 0

```
(Cell X74F74
    (CellHeader )
    (Cluster Symbols
        (Interface
            ( InterfaceUnits )
            (Port D ( InputPort ) )
            (Port CLK ( InputPort ) )
            (Port Pre ( InputPort ) )
            (Port Clr ( InputPort ) )
            (Port Q ( OutputPort ) )
            (Port QBar ( OutputPort ) ) )
        (ClusterHeader
            (Status
                (Written
                    (TimeStamp ( Date 1993 09 01 ) ( Time 16 38 19 ) )
                    (DataOrigin "ICL West Gorton" (Version "M5S083118L00") ) ) ) ) ) ) )
```

3.5 Rippers

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The ripper cell presented a major difficulty in EDIF Version 2 0 0. In the EDIF interfaces being updated, a large amount of code was dedicated to the generation of ripper descriptions. The design style of the hardware development teams using DA-X makes great use of multi-bit (arrays of) ports and nets, together with the associated bus splitting. Two special pseudo cells, split cells and merge cell are provided which facilitates the definition of very complex bus connectivity. There was not a simple one to one mapping from a split or merge cell in DA-X to a ripper cell in EDIF. The connectivity intent had to be analysed in order to determine which bits of which busses were to be associated with each other and therefore needed to be collected together into a ripper cell.

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The removal of the ripper cell has somewhat simplified the code for generating the equivalent Version 3 0 0 ripper description. which is now a connectivity object, rather than a cell. Bus connectivity in Version 3 0 0 has to be explicitly defined, thus removing the extreme difficulty in analysing the design intent through the over zealous use of Rippers.