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Report on the Viability of EDIF PCB Version (3 5 0)

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Report on the Viability of EDIF PCB Version (3 5 0)

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved by TC 217 on 1996-12-09 and endorsed by the CENELEC Technical Board on 1997-03-11.

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CENELEC
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Foreword

This technical report has been prepared by CENELEC Technical Committee TC 217, Electronic Design Automation (EDA). It was approved for publication by the CENELEC Technical Board on 1997-03-11.

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1 Introduction

The work programme of ESIP WP3 - EDIF included an activity to evaluate the viability of EDIF PCB data transfer. The EDIF standard was going through an enhancement exercise that would result in extensions that addressed the area of PCB design data transfer. Following the enhancements to the EDIF standard to include PCB design data interchange capability, trial transfers were carried out to evaluate the effectiveness of the enhancements, The ability to transfer an industry typical design successfully is of paramount importance to industry as an endorsment ot the stated capability of the enhanced standard. This report discussed the development of interfaces by the industrial partners and the subsequent transfer trials using these interfaces.
This report is divided into two sections as follows

Section 1

The development of an EDIF 350 writer carried out by Zuken-Redac written by Mike Church, Zuken-Redac. This section will by way of introduction give some background to Visula, the Zuken -Redac EDA system.The EDIF test files generated by this interface have been analysed and displayed by the EDIF development tools provided by the EDIF Technical Centre at Manchester., this exercise was carried out demonstrated the correctness of the generated EDIF and also to provide industry typical test data for validating these tools.

Section 2

The development of an EDIF 3 5 0 reader carried out by ICL written by David Hilcheson , ICL.
Some background information will be given on ICL's in-house CAD system known as DA-X. The development of the EDIF reader incorporated the EDIF Parser and Procedural Interface Kit provided by the EDIF Technical Centre.

Section 1
EDIF 3 5 0 Writer Interface from Zuken-Redac Visula EDA System

2 Background to Visula[1]

Visula is Redac Systems Limited's flagship EDA (Electronic Design Automation) system. It consists of a number of closely integrated specialist tools, and a common Informix-based Central Library of technology and parts data. The system supports all EDA design activities from initial Design Entry (Schematic Capture) right through Physical Board Layout and onto Manufacturing Outputs. The Physical Board Layout activity is centred around the Visula Layout Editor; specialist tools interact with the Layout Editor to provide best-in-class component placement, auto-routing and board simulation and analysis capabilities; the Layout Editor itself provides some rudimentary layout facilities, and forms the central control hub for managing design data.

The Visula Layout Editor can be configured so that it can deal with any of the following board technologies:

- "standard" printed circuit board (PCB);
- multi-chip module (MCM), including types C, D and L; and
- hybrid.

Since EDIF Version 3 5 0 is aimed specifically at describing printed circuit boards (and not MCMs and Hybrids), the experiment carried out during the ESIP project used only that configuration of the Visula Layout Editor that deals with the layout of printed circuit boards.

3 Visula PCB Layout Data

The data that describes a Visula PCB design consists of two major categories: library data and design data. Library data is reasonably stable (i.e. it changes infrequently) and includes parts data, technology rules, standard board stack-up definitions, component symbol data, and so on. Design data is specific to each PCB design, and is highly volatile, at least during the early phases of a design's history; design data includes component instances, routing, board outline data, and so on.

The library data that is referenced by the design data in a given design is copied into the design file. Thus it is possible to deal with the design as a complete entity in its own right (i.e. it is not necessary for the library data to be accessed in order for the design to make sense).

4 Visula Tool Integration

Figure 1 shows how the Visula PCB Layout Editor is integrated with some of the Redac-designed specialist tools, and with some of the niche-function tools supplied by other (external) parties.

The Redac-designed tools are integrated using specialised interface formats, which have been specifically tailored for the purpose. For example, PIF (Placement Interchange Format) is used to pass a subset of the design data between the PCB Layout Editor and the Redac Auto-Placement Tool, and back again. RIF is the Router Interchange Format; CIF is the Checker Interchange Format; and CAMIF is the CAM (Computer-Aided Manufacturing) Interchange Format.

The external tools are integrated using a more generic mechanism. The PCB Layout Editor is able to write and read design data described using CADIF (CAD Interchange Format), a format which is proprietary to Redac. A library of C routines called the CAD Toolkit can read a CADIF file, and access the data held within it. Using the CAD Toolkit, it is thus possible to create a software application that can translate a CADIF file into another well-defined format (e.g. NIF - Netlist Interchange Format). CADIF is both the archive format for the Visula PCB Layout Editor, and the format whereby complete or partial design descriptions can be passed onto other software tools.

Note that Figure 1 is not complete; there are many other internal and external integrations that are not shown.

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1 *Visula* is more correctly called *CAD Expert*, but most of Redac's customers and employees know the product as *Visula*.

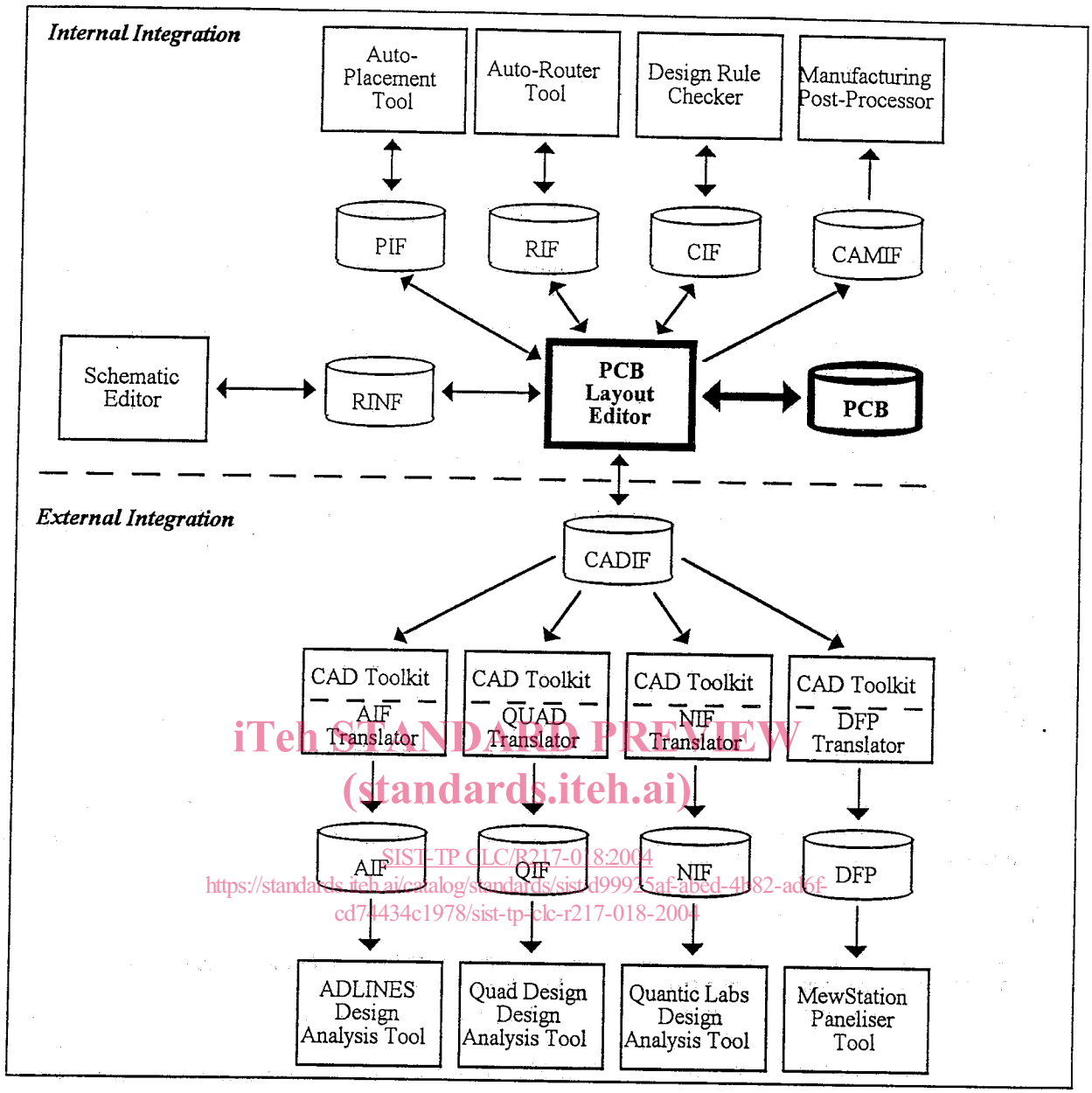

Figure 1: Visula Tool Integration

5 Background to the EDIF Experiment

The experiment with EDIF Version 3 5 0 was centred around the Visula PCB Layout Editor (since EDIF Version 3 5 0 specifically precludes MCM and Hybrid technologies). The Visula PCB Layout Editor provides extensive facilities for integration with other point tools (as explained above); the experiment took advantage of these facilities, and of work that had already taken place in creating a commercial product which had similar requirements to that of writing an EDIF file.

A new CADIF translator was created, using the CAD Toolkit. Many of the features of the CADIF-to-DFP[2] translator were appropriate for re-use (since DFP is a format which describes a printed circuit board as it is to be manufactured, as does EDIF), so the new translator was based very strongly on the original.

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2 The proprietary format which is used by MewStation, a commercially available board panelisation tool supplied by Omnimation, of San Diego, California, USA.

In order for the translator to be effective, however, a mapping between the data types contained in CADIF (which is an image of the design and library data held within a PCB design file) and EDIF was necessary.

6 CADIF to EDIF Mapping

The mapping between the data types of CADIF and EDIF proved remarkably simple. This is as a direct result of the fact that CADIF was originally designed to be as similar as possible to an early information model upon which EDIF Version 3 5 0 was eventually based. Also, the EDIF Version 3 5 0 information model was found to be very close to the information model of CADIF, thus proving that EDIF Version 3 5 0 is likely to be a close match to many other PCB CAD systems.

There were a few mismatches, however, but these were mostly in areas where it was possible to perform a transformation (from CADIF into EDIF). A prime example of this is the "padstack generator".

In the Visula PCB Layout Editor (and thus in CADIF), each of the padstacks which are used to connect component pins to the circuit board is described in terms of a "padstack generator"; this is a complex set of rules which, if followed, will produce a stack of pads. One padstack generator can give rise to many different padstacks, depending on the local circumstances. In EDIF, padstacks are described in absolute terms only. However, the Visula PCB Layout Editor can write a variant of CADIF within which padstacks are described both as padstack generators and as absolute descriptions; i.e. the complex rules which govern the creation of a padstack from its generator are carried out in the application which understands those rules.

Another place where a mismatch was found is the "teardrop". This is a special conductive structure which is placed at the junction of a route and a pad, which is such that it appears to convert a circular pad into a teardrop shape. Such items are added in order to prevent "drill bit wander" (the inherent inaccuracy of the hole drilling process) from breaking the connection of a route to a pad. In CADIF, teardrops are defined; in EDIF they are not. A CADIF teardrop had to be mapped onto an EDIF "layout shape" (an arbitrarily shaped conductor)[3].

7 Trial Transfers

Eleven separate PCB designs of varying complexity were chosen as a test set for the information transfer experiment. A number of these designs were contrived by Redac as test designs for other applications; in these cases, the designs were realistic, but of such a low complexity as to be simple to check for correctness (or error). One design was specifically created as a contrived example for the maximum coverage of EDIF concepts in the minimum size and complexity of design; this design has also been used by the EDIF community as the example design in all of the EDIF Version 3 5 0 tutorials given throughout the world. Finally, a number of real designs obtained from a number of Redac's customers (suitably doctored to protect the customers' intellectual copyright) were used in the trials.

Despite a few teething problems (due in the main to obvious syntax errors and obscure semantic errors in the generated EDIF files), the experiment proved remarkably successful. In the space of only a few weeks, a working prototype of the CADIF to EDIF translator was able to produce syntactically correct EDIF; following this, and in response to comments made from the other partners in the experiment, the translator was further improved, in order to remove some EDIF creation errors, or to add non-design information like colouring information (so that the EDIF Version 3 5 0 Visualisation System supplied by the University of Manchester could display the generated EDIF files in a multiple colours rather than plain black-and-white).

One problem found during the trials involved the interpretation of the EDIF "physical net hierarchy" principle. This is a principle which allows a hierarchy of physical design elements (e.g. routes, padstacks, footprints, etc) to carry with it a hierarchy of physical connectedness. The prototype translator actually produced syntactically and semantically correct EDIF files, in which the physical net hierarchy was not correctly carried through the padstack-toeprint-footprint hierarchy. Solving this problem in the translator has enabled the EDIF-defining community to themselves better understand and explain the physical net hierarchy.

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3 This is no problem for the process of writing EDIF Version 3 5 0 files, since the mapping is well-defined. It would cause a problem when EDIF files containing such constructs, as it would be nigh on impossible to recognise them as teardrops. This is a lack which is addressed in the new EDIF Version 3 9 9 proposal (which, if successfully balloted, will become EDIF Version 4 0 0).

The eleven example designs were numbered 1 through 10. The table in Figure 2 indicates the actual sizes of the design when expressed in CADIF and EDIF, and shows the time taken (elapsed) to translate the CADIF form to the EDIF form. Each table entry also indicates the type of design.

Note that the size of a design when expressed in CADIF is a good indicator of the design's complexity. Note too that not all of the data contained in a CADIF file will be translated into EDIF (design rule information, for example).

Design Number	Design Description	Size (CADIF) Megabytes	Size (EDIF) Megabytes	Translation Time Minutes:Seconds
1	Redac test design; 33 components; 4 layers	0.338	0.728	0:09
2	Redac test design ; 72 components; 4 layers	0.436	0.890	0:11
3	Redac test design ; 72 components; 4 layers	0.978	1.788	0:25
4	Customer design ; 261 components; 2 layers	1.129	3.006	0:43
5	Redac test design ; 30 components; 4 layers	0.211	0.325	0:04
6	Customer design ; 409 components; 10 layers	1.333	2.129	0:43
7	Customer design ; 199 components; 4 layers	1.382	1.902	0:28
8	Contrived example; for maximum EDIF concept coverage, in mimimum design size; 3 components; 4 layers	0.156	0.179	0:02
9	Customer design ; 264 components; 8 layers	1.524	2.846	0:49
10	Customer design; 616 components; 4 layers	2.698	5.087	1.:43
11	printed Circuit Design Show benchmark design(from Apple) ; 626 components; 8 layers	3.474	9.826	7:43

Figure 2: Trial Transfer Results

Figure 3 is a table showing the results of compressing the various EDIF files produced during the experiment using the standard UNIX file compression tools "compress" and "gzip" (both of which are generally available). This is an interesting table, as it shows that, although EDIF files are in themselves verbose, the compressed versions can be quite easily and efficiently transferred from place to place (via the Internet, for example).

Design Number	Size (natural) Megabytes	Size (compress) Megabytes	Size (gzip) Megabytes
1	0.728	0.107(14.7%)	0.034(4.7%)
2	0.890	0.125(14.0%)	0.042(4.7%)
3	1.788	0.303(16.9%)	0.184(10.3%)
4	3.006	0.324(10.8%)	0.143(4.8%)
5	0.325	0.061(18.8%)	0.018(5.5%)
6	2.129	0.260(12.2%)	0.095(4.5%)
7	1.902	0.253(13.3%)	0.111(5.8%)
8	0.179	0.039(21.8%)	0.014(7.8%)
9	2.846	0.304(10.7%)	0.137(4.8%)
10	5.087	0.623(12.2%)	0.341(6.7%)
11	9.826	1.044(10.6%)	0.558(5.7%)

Figure 3: EDIF File Sizes (Natural and Compressed)

As part of the testing of the CADIF to EDIF translator, Redac produced a rudimentary EDIF parser. This parser was limited in scope (due to time constraints), but it was able to check the syntax of an EDIF file, and to analyse the keyword coverage of a set of EDIF files. With this parser, it is thus possible to check how much of the EDIF Version 3 5 0 syntax is actually used in the 10 sample designs. The table in Figure 4 shows the keyword coverage figures for each of the example designs, and for the full set of sample designs; remember, though, that the keywords available in EDIF Version 3 5 0 includes those reserved for Schematic Design description (i.e. they are not applicable to PCB descriptions).

Design Number	Keyword Coverage (%)
1	26.0%
2	26.0%
3	26.2%
4	24.1%
5	26.0%
6	26.1%
7	26.1%
8	26.7%
9	26.3%
10	25.3%
11	25.5%
All	28.4%

Figure 4: EDIF Keyword Coverage