SLOVENSKI STANDARD

SIST EN 60821:1994

december 1994

IEC 60821 VMEbus – Mikroprocesorsko sistemsko vodilo za 1- do 4-bajtne podatke (IEC 60821:1991, spremenjen)

IEC 60821 VMEbus - Microprocessor system bus for 1 byte to 4 byte data (IEC 60821:1991, modified)

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Descriptors: Microprocessor systems, VMEbus

ENGLISH VERSION

IEC 821 VMEbus - Microprocessor system bus for 1 byte to 4 byte data (IEC 821:1991, modified)

Bus CEI 821 VMEbus - Bus système à microprocesseurs pour données de 1 octet à 4 octets (CEI 821:1991, modifiée)

IEC 821 VMEbus Mikroprozessor-Systembus für 1- bis 4-Byte-Daten (IEC 821:1991, modifiziert)

This European Standard was approved by CENELEC on 1993-12-08. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN 60821:1994 E

FOREWORD

The CENELEC questionnaire procedure, performed for finding out whether or not the International Standard IEC 821:1991 could be accepted without textual changes, has shown that some common modifications were necessary for the acceptance as European Standard.

The reference document, together with the common modifications prepared by the CENELEC German National Committee, was submitted to the CENELEC members for formal vote.

The text of the draft was approved by CENELEC as EN 60821 on 1993-12-08.

This European Standard replaces HD 524 S1:1989.

The following dates were fixed:

-	latest date of publication of an identical national standard	(dop)	1994-12-01
-	latest date of withdrawal of conflicting national standards	(dow)	1994-12-01

Appendices and Annexes designated "normative" are part of the body of the standard.
Appendices designated "informative" are given only for information.
In this standard, appendices A, C and D are informative and appendices B and E and annex ZA are normative.

Endorsement notice

The text of the International Standard IEC 821:1991 was approved by CENELEC as a European Standard with agreed common modifications as given below.

COMMON MODIFICATIONS

CHAPTER 0: INTRODUCTION

0.2 Replace the text of clause 0.2, Normative references, by:

NOTE: Normative references to international publications are listed in annex ZA (normative).

CHAPTER 2: IEC 821 BUS DATA TRANSFER BUS

2.2.4.5 **Replace** the **first sentence** of this paragraph by:
WRITE* is a level significant signal line that is strobed by the falling edge of the first data strobe (DSA*) and is valid as long as any data strobe (DSA* or DSB*) is low.

2.3.6 In RULE 2.65 **replace** "D08(EO) SLAVES MUST NOT respond with a falling edge on DTACK*" by "D08(O) SLAVES MUST NOT respond by driving DTACK* low".

At the end of SUGGESTION 2.8 **insert** the following text:
4) When a D08(O) SLAVE is requested to do a BYTE(0) or BYTE(2) transfer.

Replace Table 2-10 by the following table:

The following mnemonic	When applied to a	Means that it
D08(EO)	MASTER SLAVE LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Single byte read cycles: BYTE(0) READ BYTE(1) READ BYTE(2) READ BYTE(3) READ Single byte write cycles: BYTE(0) WRITE BYTE(1) WRITE BYTE(2) WRITE BYTE(3) WRITE
D08(O)	SLAVE	MUST accept the following cycles: Single byte read cycles: BYTE(1) READ BYTE(3) READ Single byte write cycles: BYTE(1) WRITE BYTE(3) WRITE
D16	MASTER SLAVE LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Double byte read cycles: BYTE(0-1) READ BYTE(2-3) READ Double byte write cycles: BYTE(0-1) WRITE BYTE(2-3) WRITE
D32	MASTER SLAVE LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Quad byte read cycles: BYTE(0-3) READ Quad byte write cycles: BYTE(0-3) WRITE

2.3.7 **Replace** the text of RULE 2.12 by:
Block transfer cycles MUST NOT cross any 256-byte boundary in the address space.

In OBSERVATION 2.87 **replace** "D08-D15" by "D00-D15".

Replace Table 2-11 by the following table:

The following mnemonic	When applied to a	Means that it
BLT	D08(EO) MASTER D08(EO) SLAVE D08(EO) LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Block read cycles: SINGLE BYTE BLOCK READ Block write cycles: SINGLE BYTE BLOCK WRITE
	D16 MASTER D16 SLAVE D16 LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Block read cycles: DOUBLE BYTE BLOCK READ Block write cycles: DOUBLE BYTE BLOCK WRITE
	D32 MASTER D32 SLAVE D32 LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Block read cycles: QUAD BYTE BLOCK READ Block write cycles: QUAD BYTE BLOCK WRITE

2.3.8 **Replace** Table 2-12 by the following Table:

The following mnemonic	When applied to a	Means that it
RMW	D08(EO) MASTER D08(EO) SLAVE D08(EO) LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Single byte read-modify-write cycles: BYTE(0) READ-MODIFY-WRITE BYTE(1) READ-MODIFY-WRITE BYTE(2) READ-MODIFY-WRITE BYTE(3) READ-MODIFY-WRITE
	D08(EO) SLAVE	MUST accept the following cycles: Single byte read-modify-write cycles: BYTE(1) READ-MODIFY-WRITE BYTE(3) READ-MODIFY-WRITE
	D16 MASTER D16 SLAVE D16 LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the following cycles: Double byte read-modify-write cycles: BYTE(0-1) READ-MODIFY-WRITE BYTE(2-3) READ-MODIFY-WRITE
	D32 MASTER D32 SLAVE D32 LOCATION MONITOR	Can generate the following cycles: MUST accept the following cycles: MUST monitor the follwing cycles: Quad byte read-modify-write cycles: BYTE(0-3) READ-MODIFY-WRITE

2.3.9 **Insert** the following NOTE after the second paragraph (before OBSERVATION 2.22):
"NOTE: Using the UAT option of the DTB protocol is only possible in a D32 environment irrespective of 16-bit or 24-bit unaligned transfers."

In Table 2-13, row B, line 3 and line 6 **replace** "Group 1, BYTE(0)" by "Group 2, BYTE(0)".

In Table 2-13, row D, line 6 **replace** "D00-D23" by "D08-D31".

In Table 2-14, row F, line 1 **replace** "D08-D15" by "D00-D07".

In Table 2-14, row F, line 2 **replace** "D16-D23" by "D08-D15".

In RULE 2.6 **replace** "D08(0)" by "D08(O)".

Replace Table 2-15 by the following table:

The following mnemonic	When applied to a	Means that it
UAT	D32 MASTER D32 SLAVE	Can generate the following cycles: MUST accept the following cycles: Quad byte read cycles: BYTE(0-3) READ Quad byte write cycles: BYTE(0-3) WRITE Triple byte read cycles: BYTE(0-2) READ BYTE(1-3) READ Triple byte write cycles: BYTE(0-2) WRITE BYTE(1-3) WRITE Double byte read cycles: BYTE(1-2) READ Double byte write cycles: BYTE(1-2) WRITE

2.3.10 In Table 2-16 **replace** "AD0" by "ADO".

2.6 In Table 2-17, 1st row **replace** "AD0" by "ADO".

In Table 2-18, row dxbs? **replace** "DRIVEN BY SLAVE" by "DRIVEN BY SLAVE?".

In Table 2-20, 1st row **replace** "AD0" by "ADO".

In Table 2-21, 1st row **replace** "AD0" by "ADO".

CHAPTER 3: IEC 821 BUS DATA TRANSFER BUS ARBITRATION

3.3.1 In line 1 of the 8th paragraph **replace** "BRO*" by "BR0*", in the next line **replace** "BGOIN*" by "BG0IN*".

3.3.2 **Replace** the text of RULE 3.14 by:
After having been granted the bus, the FAIR ARBITER MUST monitor its bus request line and it MUST NOT issue a new bus request until its bus request line has once been high.

CHAPTER 4: IEC 821 BUS PRIORITY INTERRUPT BUS

4.2.2 **Replace** the headline of clause 4.4.2 by:
Interrupt acknowledge line - IACK*

4.3 In line 3 of the first paragraph **replace** "IACK*" by "IACK".

In line 3 of the second paragraph **replace** "IACK*" by "IACK".

4.3.2 In Table 4-2, row D16, **replace** "MAY or MAY NOT" by "MAY but NEED NOT".

In Table 4-2, row ALL, **replace** twice "MAY or MAY NOT" by "MAY but NEED NOT".

4.3.7 In RULE 4.5 **replace** "has fallen" by "has been driven low".

Replace figure 4-8 by the figure given below:

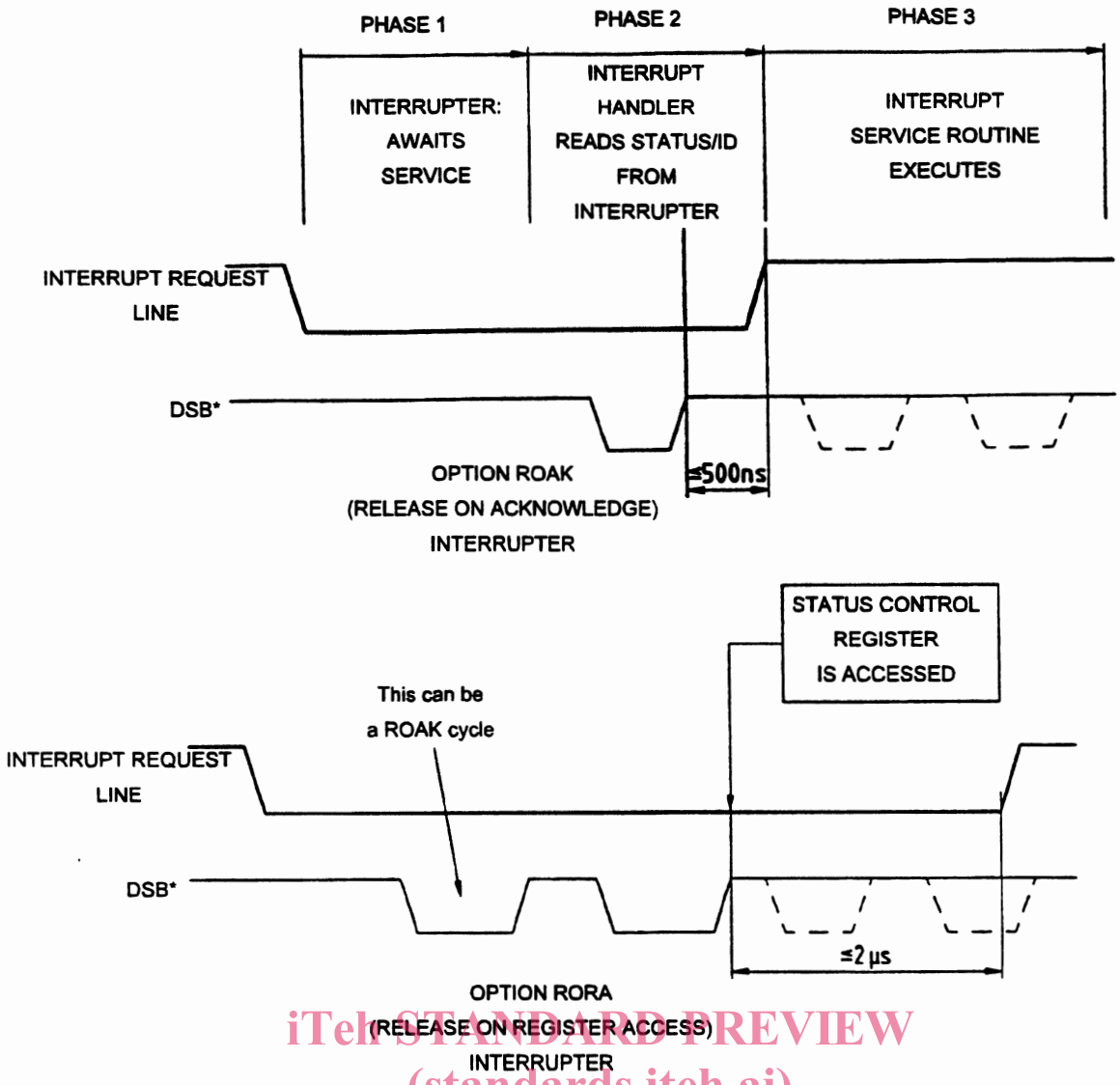


FIG. 4-8. - Release of the interrupt request lines by ROAK and RORA INTERRUPTERS.

4.3.8 In RECOMMENDATION 4.1 **delete** "and might or might not be installed in slot 1".

CHAPTER 7: IEC 821 BUS MECHANICAL SPECIFICATIONS

7.2 In RECOMMENDATION 7.1 **replace** "1.6 ± 0.2 mm (0.063 ± 0.008 in)" by "1.6 mm ± 0.2 mm (0.063 in ± 0.008 in)".

7.5.2 In RULE 7.32 **replace** "1.6 ± 0.2 mm (0.063 ± 0.008 in)" by "1.6 mm ± 0.2 mm (0.063 in ± 0.008 in)".

In RULE 7.33 **replace** "1.6 ± 0.2 mm (0.063 ± 0.008 in)" by "1.6 mm ± 0.2 mm (0.063 in ± 0.008 in)".

In PERMISSION 7.24 **replace** "J_1 or a J_2" by "J_1/J_2".

APPENDIX A GLOSSARY OF IEC 821 BUS TERMS

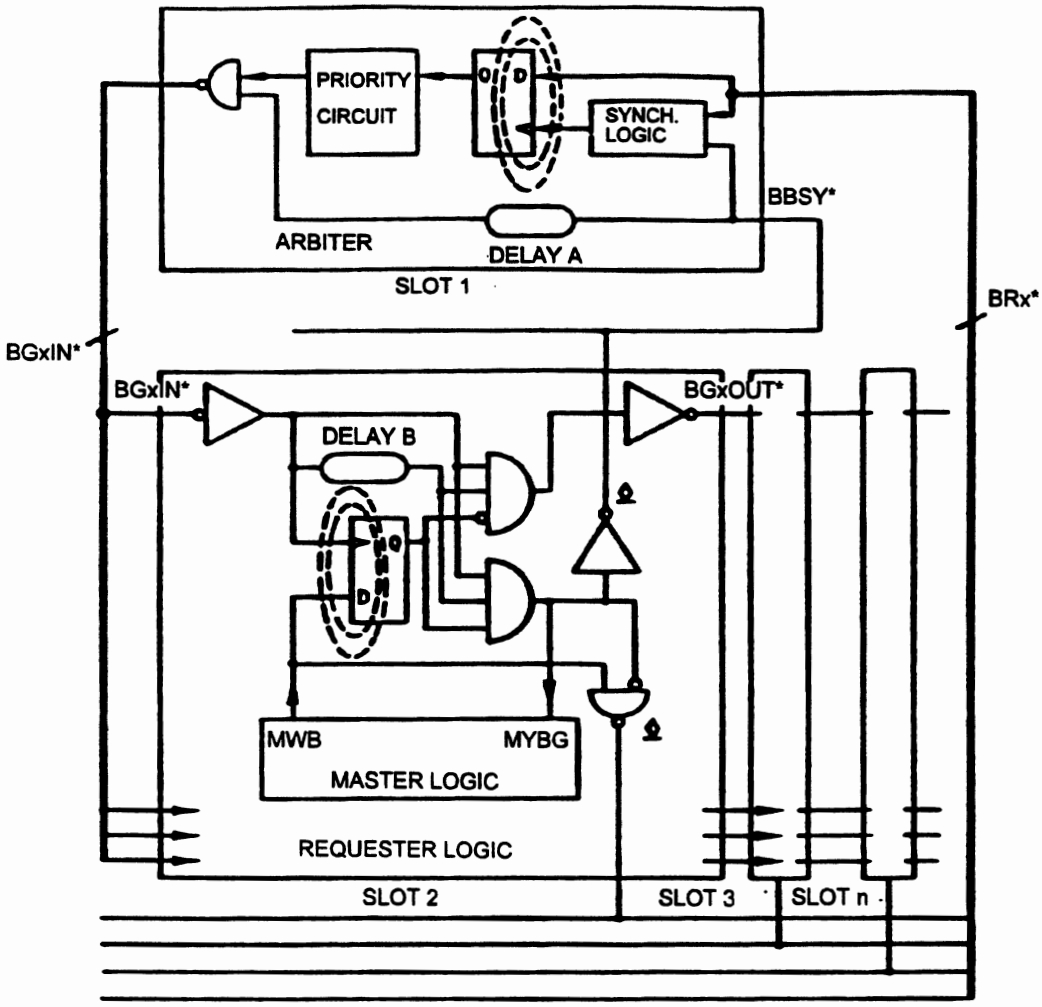
In the sixth paragraph **replace** "AD0" by "ADO".

APPENDIX D METASTABILITY AND RESYNCHRONIZATION

In the header of this appendix **replace** "APPENDIX D" by "APPENDIX D (informative)".

D.6 **Replace** figure D-5 by the following figure:

a)



b)

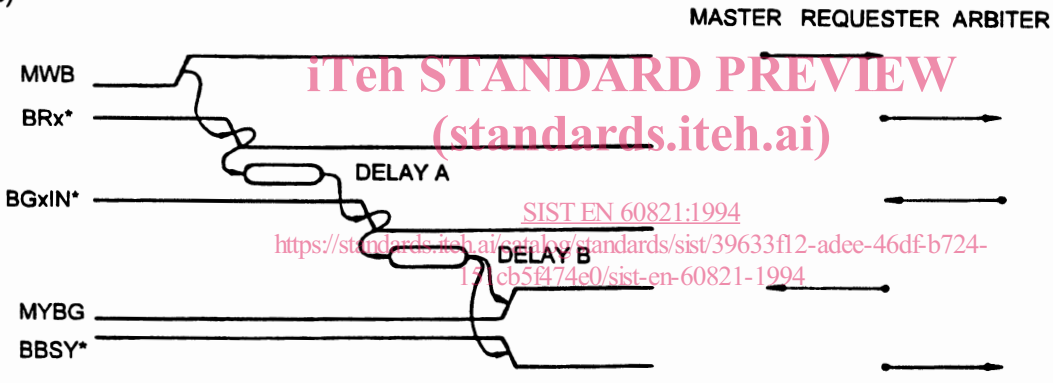


Fig. D-5. - VMEbus arbitration structure; dashed circles indicate where critical input conditions can arise
a) simplified block diagram;
b) control signals, with evidence of the handshake loop (MASTER - REQUESTER - ARBITER - REQUESTER - MASTER).

D.6.4 In line 7/8 of the second paragraph **replace** "the "PRIORITY LOGIC" block" by "the "GRANT LOGIC" block".

D.7 **Delete** the last paragraph of this clause.

APPENDIX E PERMISSIBLE CAPABILITY SUBSETS

E.2.1.2 In line 1 of the first paragraph **replace** "AD0" by "ADO".

In line 1 of the second paragraph **replace** "AD0" by "ADO".

In line 4 of the second paragraph **replace** "AD0" by "ADO".

In Table E-1 **replace** in the very right column "AD0" by "ADO".

E.2.2.4 In Table E-3, row 1, line 4 **replace** "MALL16" by "MALL8".

In Table E-4, column D08(O) **insert** "X" throughout the column.

In Table E-5, row LMRMW32, column UAT **delete** "X".

In Table E-5, row LMALL32+UAT, column UAT **insert** "X".

E.3.1 **Delete** the last sentence of the first paragraph.

ANNEX ZA (normative)

OTHER INTERNATIONAL PUBLICATIONS QUOTED IN THIS STANDARD WITH THE REFERENCES OF THE RELEVANT EUROPEAN PUBLICATIONS

When the international publication has been modified by CENELEC common modifications, indicated by (mod), the relevant EN/HD applies.

IEC Publication	Date	Title	EN/HD	Date
297-1	1986	Dimensions of mechanical structures of the 482,6 mm (19 in) series Part 1: Panels and racks	HD 493.1 S1	1988
297-3 297-3/A 1	1984 1992	Dimensions of mechanical structures of the 482,6 mm (19 in) series Part 3: Subracks and associated plug-in units	HD 493.3 S2	1993
603-2	1980	Connectors for frequencies below 3 MHz for use with printed boards Part 2: Two part connectors for printed boards, for basic grid of 2.54 mm (0.1 in), with common mounting features	-	-
822	1988	IEC 822 VSB - Parallel Sub-system Bus of the IEC 821 VMEbus	HD 576 S1	1990
823	1990	Microprocessor system bus (VMSbus) Serial subsystem bus of the IEC 821 Bus (VMEbus)	-	-

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IEC 821 VMEbus – Microprocessor system bus fir 1 byte to 4 byte data

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