SLOVENSKI STANDARD

SIST-TP CLC/R217-001:2004

september 2004

Osnovne informacije o poteku ocenjevanja podmikromilimetrske (submikronske) tehnologije CMOS

Basic information on submicron CMOS technology assessment flow

ICS 31.200

Referenčna številka
SIST-TP CLC/R217-001:2004(en)

CENELEC

R217-001

REPORT

October 1996

English version

Basic information on submicron CMOS technology assessment flow

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved by TC 217 on 1995-10-16 and endorsed by the CENELEC Technical Board on 1995-11-28.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. R217-001:1996 E

Foreword

This report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA).

It was approved by TC 217 on 1995-10-16 and approved for publication by the CENELEC Technical Board on 1995-11-28.

Contents

1 Introduction

The growing importance of electronic integrated circuits for our daily life is difficult to miss. The development, the fabrication, and the marketing of integrated circuits contribute with increasing extent to gross national products. However, the path from the first idea for an electronic circuit to operating chips is dotted with obstacles. There are for example inadequate test structures which result in misleading values for model parameters which in turn may cause faulty designed electronic circuits.

The technology assessment[1] flow (see figure 1 at page 4) outlined by this report and documented in the related documents [1, 2, 3, 4, 5] intends to establish a common base for test structures, measurement procedures, parameter extraction and verification procedures which are adequate for modern submicron silicon manufacturing technologies. This technology assessment cycle was tested with five CMOS technologies of the JESSI AC 41 project[2]. Additionally, the assessment cycle has been successfully applied to various CMOS processes outside of the JESSI project.
The generation of accurate device model parameters is the first important aspect of Technology Assessment. Another important aspect of Technology Assessment is the long-term aspect of a technology, the reliability of the technology. This topic is subject of the CENELEC documents [6, 7, 8].

Silicon manufacturers may (routinely) produce the test structures of the European Mini Test Chip. A customer searching for an appropriate technology to realize his idea for an electronic circuit will measure these test structures and extract model parameters using this technology assessment strategy. Alternatively, the customer may receive the measured data from the supplier of the technology. He can use the measured data and his data analysis programs in order to extract the model parameters. In a next step the customer simulates, for example, critical parts of his circuit using these model parameters and suitable device models. Following this path, a customer can develop the base for further decisions in a systematic way.

2 European Mini Test Chip

The European Mini Test Chip (ETC) consists of a collection of modules which can be integrated into other chip designs. Each module contains a set of test structures designed for the assessment of CMOS technologies. The individual modules can easily be rearranged according to the requirements of the actual chip design. The ETC consists of two major parts:

1. PTC - Parameter Test Chip modules (PTC). The documentation of the PTC is the task of the CENELEC document [2].

2. RTC - Reliability Test Chip modules (RTC). The RTC is documented in the CENELEC document [6].

The PTC contains CMOS transistors of various gate lengths and widths. In addition the modules provide capacitors of different geometries, resistor structures, and metal serpentine structures. The modules of the PTC were implemented, documented, and tested in five submicron CMOS technology runs during the JESSI AC 41 project. In addition, the European Mini Test Chip has been implemented into numerous CMOS technologies outside the JESSI AC 41 project.

The RTC modules contain test structures for the assessment of fundamental reliability properties like electromigration, time dependent dielectric breakdown, latch up, and hot-carrier degradation. The test structures were tested on previous test chips.

[1] The Technology Assessment Support Center (TASC) provides detailed information about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
FAX: +49-711-685-5930
E-Mail: tasc@svlsi1.mikro.uni-stuttgart.de

[2] This work is part of the JESSI Program 'Application'-Project AC 41 'Technology Assessment' and is sponsored by the national Public Authorities of Belgium, France, and Germany.

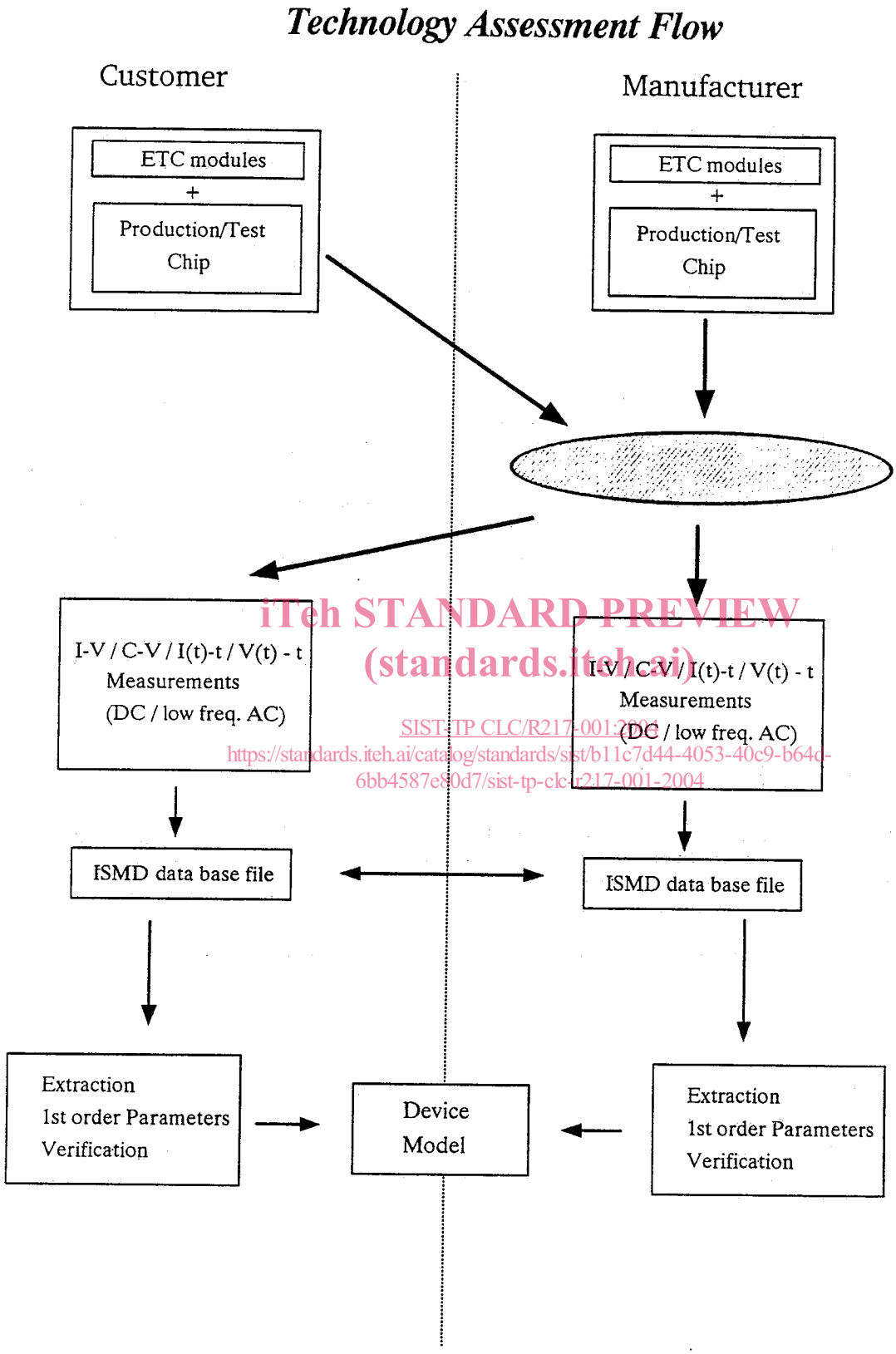

Figure 1: This diagram illustrates the technology assessment flow. The modules of the ETC are combined with other chip designs and processed. The processed chips are measured at the customer's site or at the manufacturer's site. The model parameters are extracted from the measured data. Finally the model parameters are verified.

The ETC is fully parametrized. The chip is generated automatically from the design rules of the target technology. The generation of the design rule specific ETC modules typically takes less than a day. The ETC modules can be implemented into any production or test chip. For further details see CENELEC documents [2, 6].

3 Measurements of the European Mini Test Chip

Once the design rule specific ETC modules are processed the test devices have to be measured. The measurements can be done by the manufacturer or by the customer. The measured data of the ETC modules will be stored and may be exchanged using the Interchange format for Simulated and Measured Data (ISMD). The measurements of the RTC modules consist of current-time (I-t) and/or voltage-time measurements (V-t). A detailed description of the measurements is available from CENELEC [7]. The PTC measurements consist of current-voltage (I-V) and capacitance-voltage (C-V) measurements. They include measurements of MOS capacitors, junction capacitors, the triode and the threshold region of the MOSFET, the substrate current, and the output characteristics of the MOSFET. For more information see figure 2 at page 6 and the CENELEC document [3].

3.1 Interchange Format for Simulated and Measured Data

The syntax rules of the Interchange Format for Simulated and Measured Data (ISMD) allow the creation of a compact data format. It is designed to gather the measured or simulated data which can originate from a variety of *existing* computer programs. Additionally it is a data representation format which can be read by a variety of *existing* data analysis programs with little or no modifications. It is not intended, however, to establish a data format which represents other things than measurements and their simulations

The format described by the syntax rules of ISMD allows the fast access to selected data columns of a data base file. The data and the documentation of the circumstances which lead to these data are organized in seven ISMD sections. The central section is the **data** section. The other six sections precede the data section and provide additional information about the data of the following data section(s). The preceding six sections are named **device**, **equipment**, **environment**, **info**, **outputs**, and **sources**. The syntax rules allow the handling of both table- and column-formatted data. The table format places the data of *independent* and *dependent* variables of a measurement into one table. Column-formatted files place the data of the *dependent* variable(s) of a measurement into their data sections. The size of the data sections and the total number of data sections are not limited. The up-conversion of older column-formatted data into the ISMD is straightforward.

4 JESSI $0.8\mu m$ CMOS Model

The center pieces of modern chip development are the implemented device models. Their task is the accurate *description* of the electronic devices of the integrated circuit. The most important device models are the transistor models. Basically, the implemented device model consists of three parts:

1. model equations and model parameters
2. model logic (details about implementation of logical decisions)
3. model numeric (numeric algorithms, mostly imported from system libraries)

In order to describe the transistors of submicron CMOS technologies the model equations must include at least the following physical effects:

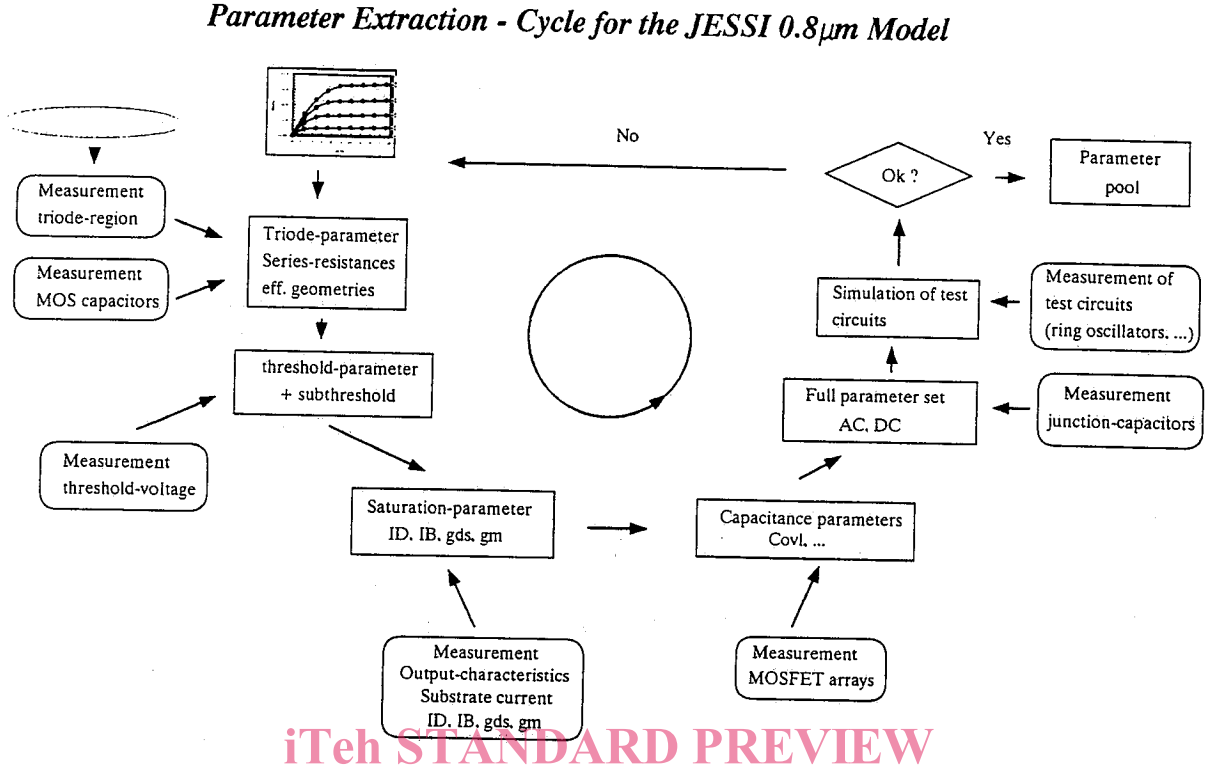

Figure 2: This diagram shows a more detailed parameter extraction cycle of the technology assessment and the corresponding measurements. The measurements are based on the test structures of the PTC.

1. short channel effects
2. narrow channel effects
3. channel length modulation
4. non-uniform impurity concentration in substrate
5. mobility reduction
6. carrier velocity saturation
7. drain/source series resistance
8. temperature effect on threshold and mobility
9. charge-based capacitances (charge conservation law)
10. substrate current model
11. Lightly doped drain (LDD) effects:
    (a) bias dependent electrical channel length
    (b) bias dependent source and drain resistances
12. Local oxidation effects (LOCOS)

The JESSI $0.8\mu m$ CMOS model includes all short and narrow channel effects and a substrate current model: special emphasis was placed on the voltage dependent effective channel length and series resistance of LDD devices. It is based on the charge-sheet approximation by Brews, including the diffusion and drift current components. To avoid discontinuities at the transitions from subthreshold to linear and from triode to saturation region, transition functions are introduced in a physical way. The model consists of only one equation, it is continuous in all regions of operation and needs no internal iteration procedures. It is implemented into at least one commercially available simulator. For further information see CENELEC document [1] and footnote 1 at page 3.

5 Parameter Extraction and Verification

Once the measurements are performed the next step consists of the extraction of the model parameters from the measured data. The results of optimization-based extraction procedures of device models which are not based on device physics often depend on the individual operator. Thus the ETC extraction procedures are mostly derived from the algebraic solutions of the equations of the physics-based device model. Examples of the extraction procedures are implemented into a commercially available parameter extraction tool and can be obtained from JESSI AC 41.

The extracted parameters include effective geometries of the MOSFET, series resistances, threshold and subthreshold parameters, saturation parameters, substrate parameters, and junction capacitance parameters as shown in figure 2 at page 6. For further details see [4].

5.1 Verification Techniques

The ETC modules contain ring oscillators which are used for the verification of the model parameters. The transistor model is used to simulate the ring oscillator frequency and currents. The difference between the measured and simulated ring oscillator data is a measure of the parameter quality. For further details see CENELEC document [4] and footnote 1 at page 3.