

SLOVENSKI STANDARD
SIST-TP CLC/R217-004:2004

01-september-2004

Model transistorja JESSI 0.8µm CMOS za simuliranje analognih in digitalnih tokokrogov

JESSI 0.8µm CMOS transistor model for analogue and digital circuit simulation

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Ta slovenski standard je istoveten z: **R217-004:1995**

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ICS:

31.080.30 Tranzistorji Transistors

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CENELEC

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RENUMBERED TITLE PAGE FOR ENGLISH VERSION

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analogue and digital circuit simulation****iTeh STANDARD PREVIEW**

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA) (former TC 117). It was approved by the Technical Committee on 1995-01-31 and endorsed by the CENELEC Technical Board on 1995-07-04.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Following decision D085/095 of the CENELEC Technical Board, all CLC/TC numbers starting from 100 have been increased by 100 to become e.g. 217.

Consequently, this technical report has been renumbered **R217-004**.

The renumbered title page is to be added to all copies of R117-004:1995.

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