SLOVENSKI STANDARD
SIST ENV 50218:2002

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Description of parameterised European mini test chip

Description of a parametrized European mini test chip

Description d'un mini composant européen paramétrisable de test

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ICS:

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Foreword

This European Prestandard has been prepared by CENELEC Technical Committee TC 217, Electronic Design Automation.

The text of the draft was submitted to the CENELEC members for comments and was approved as ENV 50218 during the CLC/TC 217 meeting on 1995-10-16.

The following date was fixed:

- latest date by which the existence of the ENV has to be announced at national level (doa) 1996-04-01

Contents

Introduction

This document is part of a series of documents describing a technology assessment cycle of submicron CMOS technologies. The series consists of six closely related documents [1, 2, 3, 4, 5] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle [1] is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS technologies is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in this document. The documentation of the measurements of these test structures is the objective of [3]. The document [4] contains the techniques used for the extraction of transistor model parameters. The purpose of document [5] is the presentation of a data exchange format which can be used with existing data evaluation programs. The test structures of the European Mini Test Chip (ETC) are developed in co-operation with the participants of the ESPRIT projects *ADCIS*, *APBB*, *CANDI*, *ACCESS* and the JESSI *Joint European Submicron Silicon Initiative* projects *Joint Logic* and *Technology Assessment*.

The test structures are implemented and verified as a part of the work of the JESSI AC 41 consortium[2]. The usefulness of the test structures of the European Mini Test Chip documented here were verified by means of three JESSI test chips. The European Mini Test Chip is processed with at least five different CMOS technologies and one BiCMOS technology of the JESSI AC 41 and JESSI Joint Logic projects. The feature sizes of the CMOS technologies range from $0.8\mu m$ down to $0.5\mu m$. The feature size of the BiCMOS technology is $0.8\mu m$. Additionally, the test structures were implemented into in-house chips which are not part of the JESSI projects. Consequently, the base of the verification of the test structures is even wider than the three (grand) JESSI test chips indicate.

1.1 Scope

This publication documents the parameterized MOS test structures of the device model **Parameter** extraction **Test Chip** (PTC) of the **European Mini Test Chip** (ETC). The devices of the PTC are a subset of the devices of the ETC. The modules of the ETC provide a minimum set of test structures used to characterize a MOS technology. The test structures of the ETC are generated automatically by a computer program for a given MOS technology. The program also generates test structures which are designed to characterize reliability aspects of a MOS technology (**Reliability Test Chip, RTC**) [6, 7, 8].

1) The Technology Assessment Support Center (TASC) provides detailed informations about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
FAX: +49-711-685-5930
E-Mail: tasc@svlsi1.mikro.uni-stuttgart.de

2) This work is part of the JESSI Program 'Application'-Project AC 41 'Technology Assessment' and is sponsored by the national Public Authorities of Belgium, France, and Germany.

Basic Modules

The modular concept of the ETC gives the possibility to arrange subsets of the modules of the ETC within Process Control Monitors (PCM) and other supplier specific test chips. The test structures of the ETC can be used as scribe lane inserts by replacing the standard pad group of the ETC (see section 2.1). The test structures of the modules of the ETC are implemented into a CAD (Computer Aided Design) program. This program is named *Parametric Test structure Generator (PTG) System*. By means of the PTG program the test structures are automatically generated for different CMOS processes and different technolgy generations. The program generates the test structures including the connections to the standard pad group by means of a rule file which contains the design rules of the give CMOS technology. The test structures generated this way can be included into any test chips. In addition, the test structures can be utilized for *scribe lane inserts*. The standard pad group has to be replaced by a special pad group which is adapted for the use with scribe lanes.

The test structures of the PTC are placed into four modules. These modules form the entire PTC and they are named *PTC1*, *PTC2*, *PTC3*, and *PTC4* according to the naming convention for standard basic modules used within the JESSI AC 41 consortium. The PTC is a part of the ETC. The transistors and resistors of the PTC are fully parameterized (see sections 3.1, 3.2, 3.3, and 3.4). The size of other test structures which are used for the extraction of process parameters is optimized to fill a given area of a module. The optimization step increases the signal strength obtained from the test structures and improves the quality of the measurement results. The actual dimensions of such structures can be obtained from the documentation file which is generated by the PTG program. This file shows the geometries of the test structures realized by a given technology.

2.1 Minimum Standard Module and Pad Group

A minimum size standard module is built up with the pad group shown in figure 1. The test structures are placed into the frame provided by the standard module. Outside, on top of the module at the left corner the name of the module is placed. The name consists of four characters. The project title is place at the right corner of the frame (see figure 1). The frame for the module is located around the pad group keeping a distance of $25\mu m$ from the pads. An edge sensor (ES) is place outside the frame at the right side of the module. The edge sensor is made of a metal bar. This sensor is used by some measurement systems which probe by means of needle cards and an edge sensor switch. The configuration of the module causes a total size of the module of $2000\mu m \times 400\mu m$. The name of each module is designed using the highest level of metal. The name of the module can be identified even on a chip with many metal layers and planarization layers.

Table 1. Basic module properties.

module name:	all modules have names with four characters
origin:	In the lower left corner of the module
size	$2000\mu m \times 400\mu m$
edge sensor:	A vertical metal bar on the right side of the module
pad group:	The pads are arranged in two rows with pitches of $200\mu m$ in a row and $200\mu m$ between the rows.
Pad shape:	octagonal
size:	$100\mu m \times 100\mu m$
metal size:	$8437\mu m^2$
passivation window:	$90\mu m \times 90\mu m$
numbering:	counter clockwise starting at the lower left corner like a dual-in-line package (refer to figure 1).
number 1:	special pad with well-contact

Table 2. Standard module (see figure 1).

Module size:	$2000\mu m \times 400\mu m$
Origin:	'O' at lower left corner of each module
Edge Sensor:	'ES'
Module name:	Name, highest level of metal

The test structures for the devices (for example transistors, resistors, etc) are parameterized. The sizes of some of the test structures are optimized to fill a fixed area of the module. This approach ensures to obtain the best signal-to-noise ratios of the measured signals.

2.2 Description of Modules PTC1 and PTC2

The modules PTC1 and PTC2 include the transistors necessary for the extraction of MOS model parameters and basic process related parameters[3, 4]. Module PTC1 contains n-channel type transistors while PTC2 includes p-channel type transistors. The devices of bothmodules are designed using equal gate geometries in order to obtain a correct basis for the comparison of the measurements and extraction results.

2.2.1 Thin Oxide Transistors

The thin oxide transistors implemented in PTC1 and PTC2 are designed according to the following definitions and rules listed in table 2.2.1. The following definitions are used:

Table 3. Definitions used for the parameterization of transistors.

lminn, lminp	Minimum allowed channel lengths (NMOS, PMOS) for the target technology. This quantity is defined by the target technology.
wminn, wminp	Minimum allowed channel widths (NMOS, PMOS) for the target technology. This quantity is defined by the target technology.
wtypn, wtypp	Typical channel width (NMOS, PMOS) for the target technology, also used in ring oscillator. This quantity is user-defined.
grid	Minimum design grid.

The parameters *wtypn* and *wtypp* are different to adapt for different driving powers in the ring oscillator. In principle, *lminn* and *lminp* as well as *wminn* and *wminp* can also be different.

The three transistors of table 2.2.1 with gate length $L = lminx$, $x = n, p$ and gate width $W = 20 \times lminx$ are intended for matching investigations.

Table 4. Dimensions. In this table the x stands for the appropriate transistor type n or p.

Transistor Number	Length (L)	Width (W)	Rotation
1	20× lminx	wminx	–
2	20× lminx	1.5× wminx	–
3	20× lminx	20× lminx	–
4	3× lminx	20× lminx	–
5	lminx +2× grid	20× lminx	–
6	lminx - grid	20× lminx	–
7	lminx	20× lminx	–
8	lminx	20× lminx	–
9	lminx	20× lminx	90 degree
10	lminx	wtypx	–
11	lminx	wminx	–

2.2.2 Thin Oxide Parallel Transistors

The 200 parallel transistors are arranged in a 25×8 array in both PTC1 and PTC2 modules. The transistor gate lengths are $L = lminx$, $x = n, p$ and the gate widths are $W = wtypx$. The transistor array is used for leakage current and also capacitance measurements.

2.2.3 Thick Oxide Transistors

Both modules PTC1 and PTC2 include thick oxide transistors with different gate materials for determination of process related parameters. The gate materials are *poly*, *metal1*, or *metal2* and are designed according to the rules of table 5:

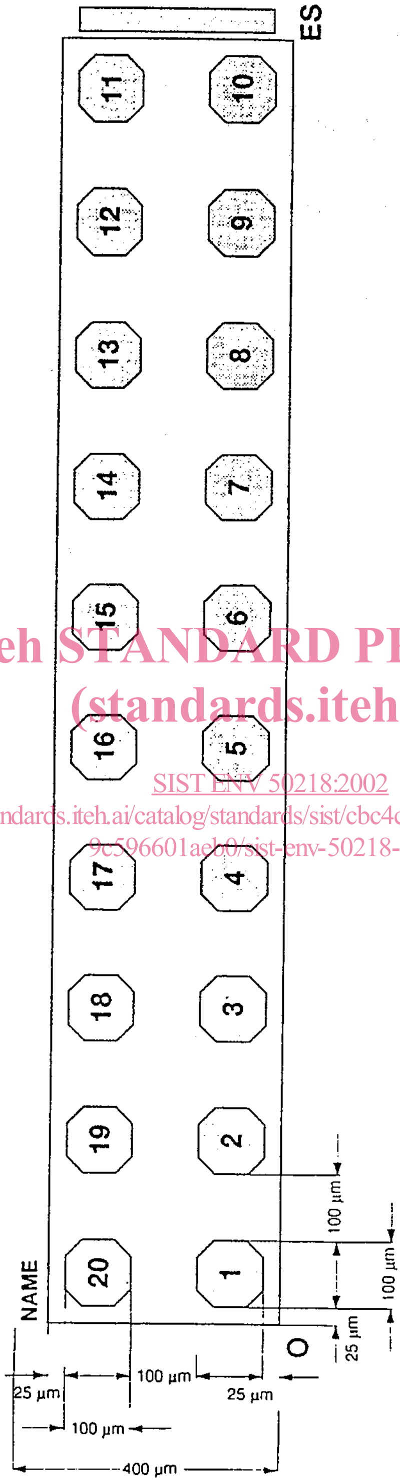
Table 5. Dimensions of thick oxide transistors.

Transistor Number	Gate Type	Length (L)	Width (W)
1	Poly	max(w(poly), s(act))	50× L
2	Metal 1	max(w(met1), s(act))	50× L
3	Metal 2	max(w(met2), s(act))	50× L

using the expressions:

w(xx) : minimum allowed width of layer (xx).
s(act) : minimum allowed space in the active area layer.

Figure 1: JESSI AC 41 Standard Pad Group



. The JESSI AC 41 standard pad group shows two rows of ten octagonal pads each. The characteristic dimensions are indicated. The character **O** denotes the origin of the Pad Group. The pads are numbered counter-clockwise.

PTC Module Configurations

3.1 PTC1 Module

The PTC1 module is of the standard size. It provides NMOS transistors utilized for model parameter extraction and for matching evaluation. The transistor array is used for leakage current and capacitance measurements. The thick oxide transistors are used for process parameter extraction. These parameters include the determination of breakdown voltage, leakage current, and thick oxide threshold voltage.

Table 6. PTC 2: NMOS transistor structures, dimensions, connections, and device names.

structure	name	gate size (width/length)	terminal	pad
common p_well	—	—	p-well	1
all transistors	—	—	source	2
all thin oxide transistors	—	—	gate	3
transistor array	—	—	gate	19
25 × 8 parallel transistors	parmos_20	1× wtypn/1× lminn	drain	20
transistor	nmos_4	1× wminn/20× lminn	drain	4
transistor	nmos_5	1.5× wminn/20× lminn	drain	5
transistor	nmos_6	20× lminn/20× lminn	drain	6
transistor	nmos_7	20× lminn/3× lminn	drain	7
transistor	nmos_8	20× lminn/$lminn + 2\times$ grid	drain	8
transistor	nmos_13	20× lminn/lminn - grid	drain	13
transistor	nmos_14	20× lminn/1× lminn	drain	14
transistor	nmos_15	20× lminn/1× lminn	drain	15
transistor (90 degree)	nmos_16	15× wminn/1× lminn	drain	16
transistor	nmos_17	1× wtypn/1× lminn	drain	17
transistor	nmos_18	1× wminn/1× lminn	drain	18
field transistors	—	—	gate	11
transistor CP	nos_fd_9	max(w[poly], s[act])/50× length	drain	9
transistor CM	m1osfd_10	max(w[met1], s[act])/50× length	drain	10
transistor CM2	m2osfd_12	max(w[met2], s[act])/50× length	drain	12

w[xxx] = minimum allowed width of layer xxx
s[act] = minimum allowed space in layer *active area*
CP = poly gate
CM = Metal 1 gate
CM2 = Metal 2 gate