INTERNATIONAL STANDARD

IEC 60748-23-1

QC 165000-1

First edition
2002-05

Semiconductor devices –
Integrated circuits –

Part 23-1:
Hybrid integrated circuits and film structures –
Manufacturing line certification –
Generic specification

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Dispositifs à semiconducteurs –
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Partie 23-1:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Spécification générique

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Consolidated editions

The IEC is now publishing consolidated versions of its publications. For example, edition numbers 1.0, 1.1 and 1.2 refer, respectively, to the base publication, the base publication incorporating amendment 1 and the base publication incorporating amendments 1 and 2.

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SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS –

Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
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International Standard IEC 60748-23-1 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-1 and the following documents:

FDIS	Report on voting
47A/638/FDIS	47A/649/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

IEC 60748-23-1 should be read in conjunction with Parts 23-2, 23-3 and 23-4.

Annex A forms an integral part of this standard.

Annex B if for information only.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This set of specifications prescribes a set of procedures to be used by users and manufacturers for the production and delivery of high-quality, special requirement hybrid integrated circuits and film structures with a specified level of quality and reliability.

This set of specifications prescribes reference criteria for the establishment, control, maintenance and development of a certified manufacturing line and represents a manufacturing line certification methodology.

The targeted level of quality and reliability is to be achieved by using best design and manufacturing practices. Examples of quality and reliability best practices for elimination of potential failure mechanisms and achievement of a targeted quality and reliability level include: material characterization for derivation of process design rules, in-process control, continuous improvement, etc.

Assessment (estimation) of the targeted quality and reliability level may be accomplished by:

a) using data obtained from the material characterization, design and process control and improvement activities; or

b) through the use of product assessment level schedule (PALS) tests.

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Part 23-2 of this set of specifications provides guidance to 'users' of hybrids in terms of the 'visual inspection standards' to be expected.

Part 23-3 of this set of specifications provides a framework for use as an assessment/audit tool to assist the suppliers, customers or an independent organization to carry out an assessment of a certified manufacturing line of a hybrid manufacturing company.

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Part 23-4 of this set of specifications provides a blank detail specification, which provides guidance to 'users' of hybrids for procurement purposes.

Part 23-5 of this set of specifications provides a means of quality assessment on the basis of qualification approval.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification

1 Scope

This set of specifications applies to high quality hybrid integrated circuits (with films) incorporating special customer quality and reliability requirements. Hybrid integrated circuits may be fully or partly completed. Partly completed devices are those that may be supplied to customers for further processing.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60027 (all parts), *Letter symbols to be used in electrical technology*

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IEC 60050 (all parts), *International Electrotechnical Vocabulary*

IEC 60068-1:1988, *Environmental testing – Part 1: General and guidance*
Amendment 1 (1992)

IEC 60748-23-1:2002
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IEC 60068-2-1:1990, *Environmental testing – Part 2: Tests – Tests A: Cold*
Amendment 1 (1993)
Amendment 2 (1994)

IEC 60068-2-2:1974, *Basic environmental test procedures – Part 2: Tests – Tests B: Dry heat*
Amendment 1 (1993)
Amendment 2 (1994)

IEC 60068-2-3:1984 (incorporating amendment 1: 1984), *Basic environmental test procedures – Part 2: Tests – Test Ca: Damp heat, steady state*
Amendment 1 (1984)

IEC 60068-2-6:1995, *Environmental testing – Part 2: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-7:1983, *Basic environmental testing procedures – Part 2: Tests – Test Ga and guidance: Acceleration, steady state*
Amendment 1 (1986)

IEC 60068-2-11:1981, *Basic environmental testing procedures – Part 2: Tests – Test Ka: Salt mist*

IEC 60068-2-14:1984, *Basic environmental testing procedures – Part 2: Tests – Test N: Change of temperature*
Amendment 1 (1986)

IEC 60068-2-17:1994, *Basic environmental testing procedures – Part 2: Tests – Test Q: Sealing*

IEC 60068-2-20:1979, *Basic environmental testing procedures – Part 2: Tests – Test T: Soldering*
Amendment 2 (1987)

IEC 60068-2-21:1999, *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*

IEC 60068-2-27:1987, *Basic environmental testing procedures– Part 2: Tests – Test Ea and guidance: Shock*

IEC 60068-2-30:1980, *Environmental testing – Part 2: Tests – Test Db: Damp heat, cyclic (12 + 12-hour cycle)*
Amendment 1 (1985)

IEC 60068-2-44:1995, *Environmental testing – Part 2: Tests – Guidance on Test T: Soldering*

IEC 60068-2-45:1980, *Basic environmental testing procedures – Part 2: Tests – Test XA and guidance: Immersion in cleaning solvents*
Amendment 1 (1993)

IEC 60068-2-47:1999, *Environmental testing – Part 2-47: Tests – Mounting of components, equipment and other articles for vibration, impact and similar dynamic tests*

IEC 60068-3 (all parts) *Environmental testing procedures – Part 3: Supporting documentation and guidance*

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IEC 60068-3-4:2001, *Environmental testing – Part 3-4: Supporting documentation and guidance – Damp heat tests*

IEC 60748-23-1:2002
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IEC 60068-5 (all parts), *Environmental testing – Part 5: Guide to drafting of test methods*

IEC 60134:1961, *Rating systems for electronic tubes and valves and analogous semiconductor devices*

IEC 60191-2:1996, *Mechanical standardization of semiconductor devices*

IEC 60617 (all parts), *Graphical symbols for diagrams*

IEC 60695-2-2:1991, *Fire hazard testing – Part 2: Test methods – Section 2: Needle-flame test*
Amendment 1 (1994)

IEC 60747-1:1983, *Semiconductor devices – Discrete devices – Part 1: General* [1]
Amendment 3 (1996)

IEC 60748-1, *Semiconductor devices – Integrated circuits – Part 1: General* [2]

IEC 60748-23-2:2002, *Semiconductor devices – Integrated circuits – Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests*

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1 Together with any other part of IEC 60747 or IEC 60748 relevant to the specific hybrid application, including terminology.

2 To be published.

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Manufacturers' self-audit checklist and report*

IEC 60749:1996, *Semiconductor devices – Mechanical and climatic test methods* [3]
Amendment 1 (2000)
Amendment 2 (2001)

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

ISO 1000:1992, *SI units and recommendations for use of their multiples and of certain other units*
Amendment 1 (1998)

ISO 9000:2000, *Quality management systems – Fundamentals and vocabulary*

ISO 2859 (all parts), *Sampling procedures for inspection by attributes*

IECQ 001002-3:1998, *IEC Quality Assessment System for Electronic Components (IECQ) – Rules of Procedure – Part 3: Approval procedures*

IECQ 001005:2000, *Register of Firms, Products and Services approved under the IECQ System, including ISO 9000*

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3 Definitions

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For the purpose of this part of IEC 60748, the units, graphical symbols, letter symbols and terminology given in IEC 60027, IEC 60050, IEC 60617, IEC 60747-1, IEC 60748-1 and ISO 1000, as well as the following definitions, shall apply.

3.1
added component
component added to a hybrid film integrated circuit that is not formed on the surface of the substrate

NOTE Added components are incorporated components (see 4.1.3 of IECQ 001002-3) excluding those formed on the substrate.

3.2
burn-in
non-destructive procedure designed to screen out early lifetime failures

NOTE Burn-in is an accelerated conditioning with a device under its operating electrical load at an elevated temperature, which is generally the maximum operating temperature that does not exceed the thermal rating of the device.

3.3
capability qualifying component (CQC)
test specimen used to assess, in part or in whole, a declared capability

NOTE It may be either a specially designed test specimen (process test vehicle) or a normal production circuit (qualification circuit), or a combination of both.

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[3] There exists a consolidated edition 2.2 (2002) that includes edition 2.0 (1996), its amendment 1 (2000) and amendment 2 (2001).

3.4
category dissipation
fraction of the rated dissipation defined in the detail specification, applicable at the upper category temperature taking account of the derating curve

NOTE Prescribed (where appropriate) in the detail specification.

3.5
certified manufacturing line
manufacturing line which is formally qualified and in which a manufacturer defines a basic technology and technology flow which can be used to produce a range of different components

NOTE The defined technology flow covers all processes from initial component design to the final completion of tested components ready for delivery.

3.6
custom designed
qualifying term for a circuit manufactured to a specific customer's requirements

3.7
electrical endurance
procedure similar to burn-in but of extended duration. Electrical endurance may be considered destructive or non-destructive dependent upon duration and severity

3.8
film circuit element
circuit element consisting of a film or films

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3.9
lower category temperature (LCT)
minimum ambient temperature ($T_{amb\ min}$) at which a circuit has been designed to operate continuously

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3.10
measurement uncertainty
statement of the limits of the range within which the true value of the measurement is expected to lie in relation to the recorded result, with a defined confidence level

3.11
part-finished
a film integrated circuit or hybrid film integrated circuit taken uncompleted from a production line

NOTE It cannot be completely assessed to the specification applicable in its normal finished state.

3.12
package
total or partial envelope of an integrated circuit which provides:

– mechanical protection

– environmental protection

– outline dimensions

NOTE The package may also contain or provide terminals. It contributes to the thermal characteristics of the integrated circuit.

3.13
primary stage of manufacture
production of the first film layer of a film integrated circuit on the surface of a substrate

3.14
process test vehicle (PTV)
device or test structure used to verify, analyze or monitor processes or electrical/physical attributes

3.15
product assessment level schedules (PALS)
minimum circuit process and test requirements for the different market sectors/operating environments (see annex A)

3.16
qualification circuit (QC)
circuit which is representative of circuits manufactured to declared and identical processes and used for approval tests to one of the product assessment level schedules (PALS)

3.17
repair
making good of an approved circuit which has been damaged or has become defective after release

NOTE Circuits which have been repaired should not be released under the IECQ system.

3.18
rework
reprocessing or corrective processing operation carried out on a circuit before release to the customer

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3.19
screening
examination or testing applied to all products in a lot for the purpose of detecting and removing potential failures

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3.20
upper category temperature (UCT)
maximum ambient temperature ($T_{amb\ max}$) at which a circuit has been designed to operate continuously at that portion of the rated dissipation which is indicated in the category dissipation

4 Standard and preferred values

Where practical, values should be selected from the following:

a) dimensions: IEC 60191-2;

b) temperatures in degrees Celsius (°C):

–65, –55, -40, –25, –10, 0, +5, +25, +40, +55, +70, +85, +100, +125, +150.

5 Marking

5.1 Circuit

The marking of the circuit shall be specified in the detail specification and provide adequate circuit identification and traceability. As space permits it shall include:

a) terminal identification (e.g. position of pin No.1);

b) type designation;

c) date code;

e) handling precautions;

f) mark of conformity;

g) manufacturer's name or trade mark;

h) serial number;

i) product assessment level schedule (PALS) number.

5.2 Despatch primary pack

The marking of the despatch primary pack shall be specified in the detail specification and shall provide adequate contents identification and traceability. It should include, as relevant, information from 5.1 and the following:

a) certificate of conformity reference number;

b) order or contract number;

c) quantity of circuits.

6 Quality assessment procedures

6.1 General

6.1.1 Eligibility for manufacturing line certification

Manufacturing line certification may be granted only to a manufacturer of film integrated circuits and/or hybrid film integrated circuits who has been granted manufacturer's approval in accordance with the requirements of ISO 9000, as detailed in clause 2 of IEC QC 001002-3. A manufacturer is eligible for manufacturing line certification if direct supervision by the designated management representative (DMR), or in the case of subcontracted processes, the local DMR, is applied to the manufacturing process including the "primary stage" of manufacture. The DMR shall ensure the proper and effective co-ordination and control of certified manufacturing line through the formation of a senior management team.

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6.1.2 Subcontracting

Subcontracting shall be in accordance with the requirements of 4.2.2 of IEC QC 001002-3.

The subcontracted manufacturing processes may be either:

a) film production;

b) trimming of elements;

c) mounting of components;

d) packaging;

e) others.

Not more than two of the four named processes shall be subcontracted.

6.1.3 Control of procurement sources and incoming material

Subclause 4.2.3 of IEC QC 001002-3 applies with the following details:

6.1.3.1 Added components, part finished components, materials and subcontracted processes covered by a IECQ specification

These shall be procured using the normal IECQ release procedures. Under these conditions no other assessment is required.

6.1.3.2 Added components, part finished components, materials and subcontracted processes not covered by a IECQ specification

The DMR shall:

a) ensure the existence of a procurement specification under his control.

b) perform an evaluation programme for each procured item or family from all manufacturing sources in accordance with the relevant product assessment level schedules (PALS) for the finished circuit (see annex A).

   This evaluation programme may be carried out as part of the initial design evaluation. Each variant shall be submitted to the minimum sample size and acceptance criteria in the appropriate PALS. Structural similarity principles may be used.

c) define and institute a goods inward inspection and a continuous vendor rating system for all such items.

d) instigate such other procedures as are necessary to ensure that procurement is equivalent to any relevant IECQ release.

6.1.4 Validity of release for delivery

6.1.4.1 General

Circuits may be released under manufacturing line certification subject to the following conditions:

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a) The circuits have been designed and manufactured within the manufacturer's approved capability.

b) An evaluation programme has been performed for each circuit or family in accordance with the relevant PALS for the finished circuit. These PALS, which are listed in annex A, are the minimum product release requirements of IEC 60748-23-1 to IEC 60748-23-5. Each level specifies the minimum assessment requirement and process requirements. However, customers are at liberty to add to the testing requirements or put the design evaluation requirement on a periodic product sampling basis. The structural similarity claims, where applicable for each product, are to be agreed between the customer and manufacturer. The product assessment level of release is to be clearly shown on the detail product specification and the certificate of conformity. The device screening sequence shown in each PALS is mandatory except that, when agreed by customer and manufacturer, the sequence of sealing and final electrical test may be reversed. For design evaluation there is no requirement for sequence of testing and different samples may be used for each test. The manufacturer may, however, at his risk, use the same samples for any or all of the tests in the design evaluation section. It is necessary that devices used for device sample testing or design evaluation shall have successfully completed device screening. Where a per cent defective allowable (PDA) is required for a screening sequence, the PDA is calculated at the beginning of the burn-in test. Tests performed before burn-in, or after the electrical test at T_{amb} which immediately follows the burn-in, are not subject to PDA. Where the number of defectives allowed by the PDA in any lot is not a whole number, the allowance shall be rounded up to the next whole number. In the event of a failure at PDA, if the per cent defective is found to be greater than the PDA but not greater than twice the PDA, the devices which passed may be resubmitted to burn-in once only and examined to a tightened PDA. The tightened PDAs are 10 % ⇒ 7 %, 7 % ⇒ 5 % and 5 % ⇒ 3 %.

c) The circuits, their added components, piece parts and materials are traceable to original manufacturer's lot numbers.

6.1.4.2 Release of circuits subjected to destructive or non-destructive tests

Circuits subjected to destructive (D) mechanical or environmental tests shall not be included in the lot for delivery.

Circuits subjected to non-destructive (ND) tests may be delivered, provided they meet the requirements of the detail specification.

6.1.4.3 Delayed deliveries of circuits

Circuits held for a period exceeding two years following release of the lot shall be retested to the electrical and solderability tests of the detail specification, prior to delivery, unless a longer period can be demonstrated by the manufacturer.

6.1.5 Rework

6.1.5.1 General

Rework shall only be permitted within the procedures declared in the manufacturer's declared procedures as defined in 4.7.1 of IEC QC 001002-3.

A customer may prohibit or restrict rework on circuits to be supplied to a particular contract.

6.1.5.2 General requirements

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a) where circuits have been directly embedded in hard plastic encapsulants, no rework is permitted other than that specified in 6.1.5.8;
b) maximum time/temperature excursions during rework shall be specified;
c) screening, adequate to test the rework in accordance with the manufacturer's declared procedures, shall be carried out after rework.

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6.1.5.3 Film conductors

Film conductors may be reworked by the attachment of conducting links provided that the number of links and methods of attachment comply with the requirements of the manufacturer's declared procedures.

6.1.5.4 Wire bonds

Rebonding to the semiconductor die shall be attempted only once and rebonding is restricted to not more than 10 % of the wire bonds in a circuit. The rebonds shall be on at least 50 % undisturbed metallization (excluding probe marks).

Rebonding to header pins and film conductor tracks is not restricted except that each rebond is on at least 50 % undisturbed metallization.

6.1.5.5 Compound wire bonds

The placing of one wire bond on top of another wire (compound wire bond) is permitted except on the semiconductor die. The new bond shall cover at least 75 % of the original bond, and shall be attempted only once.

6.1.5.6 Added components

Added components may be replaced up to two times except for a eutectic bonded semiconductor die which may be replaced only once, unless demonstrated otherwise by the manufacturer.