INTERNATIONAL STANDARD

IEC 60748-23-2

QC 165000-2

First edition
2002-05

Semiconductor devices –
Integrated circuits –

Part 23-2:
Hybrid integrated circuits and film structures –
Manufacturing line certification –
Internal visual inspection and special tests

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Dispositifs à semiconducteurs –
Circuits intégrés –

Partie 23-2:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Contrôle visuel interne et essais spéciaux

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

FOREWORD

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International Standard IEC 60748-23-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-2 and the following documents:

FDIS	Report on voting
47A/639/FDIS	47A/650/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

IEC 60748-23-2 should be read in conjunction with Parts 23-1, 23-3 and 23-4.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This set of specifications prescribes a set of procedures to be used by users and manufacturers for the production and delivery of high-quality, special requirement hybrid integrated circuits and film structures with a specified level of quality and reliability.

This set of specifications prescribes reference criteria for the establishment, control, maintenance and development of a certified manufacturing line and represents a manufacturing line certification methodology.

The targeted level of quality and reliability is to be achieved by using best design and manufacturing practices. Examples of quality and reliability best practices for elimination of potential failure mechanisms and achievement of a targeted quality and reliability level include: material characterization for derivation of process design rules, in-process control, continuous improvement, etc.

Assessment (estimation) of the targeted quality and reliability level may be accomplished by:

a) using data obtained from the material characterization, design and process control and improvement activities; or

b) through the use of product assessment level schedule (PALS) tests.

Part 23-1 of this set of specifications provides general information.

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Part 23-3 of this set of specifications provides a framework for use as an assessment/audit tool to assist the suppliers, customers or an independent organization to carry out an assessment of a certified manufacturing line of a hybrid manufacturing company.

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Part 23-4 of this set of specifications provides a blank detail specification, which provides guidance to 'users' of hybrids for procurement purposes.

Part 23-5 of this set of specifications provides a means of quality assessment on the basis of qualification approval.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

1 Scope

This part of IEC 60748 applies to high quality approval systems for hybrid integrated circuits and film structures.

The purpose of the tests is to perform visual inspections on the internal materials, construction and workmanship of hybrid, multichip and multichip module microcircuits and passive elements used for microelectronic applications including r.f./microwave.

These tests are for both Class H and Class K quality levels, SAW and film hybrid/multichip/ multichip module microcircuits using substrates such as ceramic and silicon. Class K is applicable to all microcircuits released to product assessment level schedule 11 (e.g. for space applications – see IEC 60748-23-1). Class H is applicable to all other microcircuits released to this standard. The following types of microcircuits may be inspected:

a) passive thin and thick film networks;

b) active thin and thick film circuits;

c) multiple circuits, including combinations, stacking or other interconnections of 1 a) and 1 b).

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Where the deposited film has geometric features larger than 25 µm, the inspection criteria defined in clause 5 apply. In cases where deposited features are smaller than this (e.g. deposited integrated circuits) the inspection requirements of IEC 60747 shall be applied.

These tests will normally be used on microelectronic devices prior to capping or encapsulation to detect and eliminate devices with internal non-conformances that could lead to device failure in normal application. They may also be employed on a sampling basis to determine the effectiveness of the manufacturers' quality control and handling procedures.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary*

IEC 60747-1:1983, *Semiconductor devices – Discrete devices – Part 1: General* [1]

Amendment 3 (1996)

IEC 60748-1, *Semiconductor devices – Integrated circuits – Part 1: General* [1]

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

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[1] Together with any other part of IEC 60747 or IEC 60748 relevant to the specific hybrid application, including terminology.

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Manufacturers' self-audit checklist and report*

IEC 60748-23-4:2002, *Semiconductor devices – Integrated circuits – Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification*

IEC 61191-2:1998, *Printed board assemblies – Part 2: Sectional specification – Requirements for surface mount soldered assemblies*

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

EN 100012:1995, *Basic Specification: X-ray inspection of electronic components*

3 Definitions

For the purpose of this part of IEC 60748, the definitions given in IEC 60050, IEC 60747, IEC 60748-1 and IEC 60748-23-1, as well as the following definitions, shall apply.

3.1
active circuit area
includes all areas of functional circuit elements, operating metallization or connected combinations thereof excluding beam leads; in the case of resistors, includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads)

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3.2
add-on substrate
supporting structural material into and/or upon which glassivation, metallization and circuit elements are placed and the entire assembly is in turn placed on and attached to the main substrate

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3.3
attachment medium
material used to effect the attachment of an element to an underlying surface (e.g. adhesive, solder, alloy)

3.4
blister, metallization
hollow bump that can be flattened

3.5
block resistor
solid, rectangularly shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements

3.6
bonding pad
metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element

3.7
bonding site
metallized area on a substrate or element intended for a wire or ribbon interconnecting bond

3.8
bridging
complete connection between circuit features not intended to be connected

3.9
cold solder joint
solder joint whose appearance is "grainy" or "dull"

NOTE Where a "grainy" or "dull" appearance is characteristic of certain solder materials (e.g. AuSn, etc.), this criterion should not cause these materials to be rejected.

3.10
compound bond
one bond on top of another

3.11
conductive attach
process and materials used for the attachment that also provides an electrical contact or thermal dissipation path (e.g. solder, eutectic, solder-impregnated epoxy)

3.12
conductive substrate
substrate that can conduct electricity

NOTE Copper or doped silicon, for example, are conductive substrates while alumina and quartz are non-conductive (insulating) substrates.

3.13
contact window
opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate

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3.14
controlled environment
environment that is in accordance with the requirements of the appropriate product assessment level schedules (PALS) in Annex A of IEC 60748-23-1 and with respect to cleanroom class and (where specified) temperature and relative humidity

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3.15
corrosion
gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product

3.16
coupling (air) bridge
raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material

3.17
crazing
presence of numerous, minute, interconnected surface cracks

3.18
crossover
transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing

3.19
detritus
fragments of original or trim-modified resistor or conductor material

3.20
dielectric
insulating material that does not conduct electricity but may be able to sustain an electric field

NOTE It can be used in crossovers, as a passivation or a glassivation, or in capacitors.

3.21
dielectric attach
process and materials used for attachment that does not provide electrical contact or thermal dissipation

3.22
edge metallization
metallization that electrically connects the metallization from the top surface to the opposite side of the substrate

3.23
element
constituent of a hybrid microcircuit; such as integral deposited or screened passive elements, substrates, discrete or integrated electronic parts including dies, chips and other microcomponents; also mechanical piece parts such as cases and covers; all contributing to the operation of a hybrid microcircuit

3.24
electrically common
satisfied when two or more conductive surfaces or interconnects are of equal d.c. voltage/signal potential

3.25
end terminated or wrap-around elements
those elements which have electrical connections on the ends (sides) and/or base of their bodies

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3.26
foreign material
any material that is foreign to the element or microcircuit or any non-foreign material that is displaced from its original or intended position in the element or microcircuit package

NOTE It is considered attached when it cannot be removed by a nominal gas blow (approximately 138 kN/m^2) (20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of colour fringing around the periphery of the particle.

3.27
glassivation
top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads

NOTE Crazing is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.

3.28
insulating layer
dielectric layer used to isolate single or multilevel conductive and resistive material or to protect top level conductive resistive material

3.29
intermetallics (purple plague)
one of several gold-aluminium compounds formed when bonding gold to aluminium and activated by re-exposure to moisture and high temperature (> 340 °C)

NOTE Purple plague is purplish in colour and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.