

INTERNATIONAL STANDARD

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2002-05

Semiconductor devices – Integrated circuits –

Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

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*Dispositifs à semiconducteurs –
Circuits intégrés –*

*Partie 23-2:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Contrôle visuel interne et essais spéciaux*



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CONTENTS

FOREWORD	7
INTRODUCTION	9
1 Scope	10
2 Normative references.....	10
3 Definitions	11
4 Apparatus	18
5 Procedure.....	18
5.1 General	18
5.2 Sequence of inspection.....	19
5.3 Inspection control	19
5.4 Re-inspection	19
5.5 Exclusions	19
5.6 Magnification	19
5.7 Format and conventions	19
5.8 Interpretations	20
6 Thin film element inspection	20
6.1 Operating metallization non-conformances – "high magnification"	20
6.2 Passivation non-conformances "high magnification"	26
6.3 Glassivation non-conformances, "high magnification"	27
6.4 Substrate non-conformances "high magnification"	28
6.5 Foreign material non-conformances "low magnification"	30
6.6 Thin film resistor non-conformances, "high magnification"	31
6.7 Laser trimmed thin film resistor non-conformances, "high magnification"	36
6.8 Multilevel thin film non-conformances, "high magnification"	45
6.9 Coupling (air) bridge non-conformances "high magnification"	45
7 Planar thick film element inspection	47
7.1 Operating metallization non-conformances "low magnification"	47
7.2 Substrate non-conformances, "low magnification"	51
7.3 Thick film resistor non-conformances, "low magnification"	54
7.4 Trimmed thick film resistor non-conformances, "low magnification"	56
7.5 Multilevel thick film non-conformances, "low magnification"	58
7.6 All thin film capacitors and overlay capacitors used in GaAs microwave devices, "low magnification"	59
8 Active and passive elements.....	59
9 Element attachment (assembly), "magnification 10× to 60×".....	59
9.1 Solder connections (general appearance).....	59
9.2 Element attachment requirements.....	60
9.3 Leaded and leadless element attachment	64
9.4 Dual-in-line integrated circuit attachment (butt joints)	64
9.5 Axial and radial leaded components (lap joints)	67
9.6 Components with feet (combined butt and lap joints)	68
9.7 Leadless chip carriers.....	70
10 Element orientation.....	71
11 Separation	71

12	Bond inspection, magnification 30× to 60×	72
12.1	Ball bonds	72
12.2	Wire wedge bonds	72
12.3	Tailless bonds (crescent)	73
12.4	Compound bond	73
12.5	Beam lead	74
12.6	Mesh bonding	76
12.7	Ribbon bonds	76
12.8	General	77
13	Internal leads (e.g. wires, ribbons, beams, wire loops, ribbon loops, beams, etc.), "magnification 10× to 60×"	77
14	Screw tabs and through-hole mounting, magnification 3× to 10×	78
15	Connector and feedthrough centre contact soldering, magnification 10× to 30×	78
16	Package conditions, solder assemblies, lead frame attachments, conformal coating, "magnification 10× to 60×"	81
16.1	Package conditions	81
16.2	Lead frame attachment	81
16.3	Conformal coating	84
17	Non-planar element inspection	84
17.1	General non-planar element non-conformances, "low magnification"	84
17.2	Foreign material non-conformances "low magnification"	85
17.3	Ceramic chip capacitor non-conformances "low magnification"	85
17.4	Tantalum chip capacitor non-conformances, "low magnification"	88
17.5	Parallel plate chip capacitor non-conformances, "low magnification"	88
17.6	Inductor and transformer non-conformances, "low magnification"	89
17.7	Chip resistor non-conformances, "low magnification"	90
18	Surface acoustic wave (SAW) element inspection	92
18.1	Operating metallization non-conformances "low magnification"	92
18.2	Substrate material non-conformances "low magnification"	92
18.3	Foreign material non-conformances "low magnification"	92
19	Summary	93
20	Radiographic inspection	93
20.1	Requirements	93
21	Particle impact noise detection (PIND) test	95
21.1	General	95
21.2	Equipment	95
21.3	Test procedure	96
21.4	Failure criteria	96
21.5	Lot acceptance	96
21.6	The detail specification	97
	Figure 1 – Class H – Metallization scratch criteria	14
	Figure 2 – Class H – Metallization scratch criterion	21
	Figure 3 – Class H – Metallization width reduction at bonding pad criterion	21
	Figure 4 – Class K – Metallization width pad reduction at bonding pad criterion	21
	Figure 5 – Class H – Metallization void criterion	22
	Figure 6 – Class H – Interdigitated capacitor metallization void criterion	23

Figure 7 – Class K – Interdigitated capacitor metallization void criterion.....	23
Figure 8 – Class H – Operating metallization protrusion criterion	24
Figure 9 – Class H – Interdigitated capacitor metallization protrusion criterion	24
Figure 10 – Class H – Metallization alignment criterion	25
Figure 11 – Class K – Metallization alignment criterion	25
Figure 12 – Class H – Wrap-around connection unmetallized area criterion	26
Figure 13 – Class H – Passivation non-conformance criteria	26
Figure 14 – Class H – Laser trimmed glassivation non-conformance criteria	27
Figure 15 – Class H – Separation and chipout criteria	29
Figure 16 – Class H – Crack criteria.....	29
Figure 17 – Class K – Semicircular crack criterion.....	30
Figure 18 – Class H – Film resistor width reduction at terminal by voids criterion	31
Figure 19 – Class H – Film resistor width reduction at terminal by necking criterion	32
Figure 20 – Class H – Resistor width reduction by voids and scratches criteria	32
Figure 21 – Class H – Metal/resistor overlap criterion	33
Figure 22 – Class H – Contact overlap criterion	33
Figure 23 – Class H – Resistor separation criteria.....	34
Figure 24 – Class H – Substrate irregularity criterion	34
Figure 25 – Class H – Resistor width increase criterion.....	35
Figure 26 – Class H – Protrusion of resistor material criterion	35
Figure 27 – Class H – Bridging of resistor material criteria	36
Figure 28 – Class H – Kerf width criteria	37
Figure 29 – Class H – Detritus criterion for self-passivating resistor materials.....	37
Figure 30 – Class H – Resistor loop element detritus criterion for self-passivating resistor materials	38
Figure 31 – Bridging of detritus between rungs in the active area of a resistor ladder structure criterion.....	38
Figure 32 – Class H – Resistor ladder structure nicking and scorching criteria exceptions	39
Figure 33 – Class H – Resistor loop nicking and scorching criteria exceptions	40
Figure 34 – Class H – Laser nicking criteria exception for the last rung of a resistor ladder	40
Figure 35 – Class H – Resistor ladder sidebar trim criterion	41
Figure 36 – Class H – Laser trim misalignment criteria	41
Figure 37 – Class H – Laser trim kerf extension into metallization criteria	42
Figure 38 – Class H – Resistor width reduction at metallization interface criteria.....	42
Figure 39 – Class H – Resistor width reduction by trimming criteria	43
Figure 40 – Class H – Resistor width reduction and untrimmed resistor material criteria	44
Figure 41 – Class H – Laser trim pitting criterion.....	44
Figure 42 – Class H – Insulating material extension criteria	45
Figure 43 – Class H and Class K – Coupling (air) bridge criteria	46
Figure 44 – Class H – Metallization scratch criteria	47
Figure 45 – Class H – Metallization width reduction at bonding pad criteria.....	48
Figure 46 – Class K – Metallization width reduction at bonding pad criteria.....	48

Figure 47 – Class H – Metallization void criteria	48
Figure 48 – Class H – Metallization protrusion criterion	50
Figure 49 – Class H – Metallization overlap criterion	50
Figure 50 – Class H – Wrap-around connection unmetallized area criterion	51
Figure 51 – Class H – Separation and chipout criteria	52
Figure 52 – Class H – Additional crack criteria	52
Figure 53 – Class K – Semicircular crack criterion	53
Figure 54 – Class H – Resistor width reduction at terminal caused by voids criterion	54
Figure 55 – Class H – Resistor width reduction at terminal by neck-down criterion	54
Figure 56 – Class H – Resistor width reduction criteria	55
Figure 57 – Class H – Resistor overlap criterion	55
Figure 58 – Class K – Resistor overlap criterion	55
Figure 59 – Resistor overlap criterion	56
Figure 60 – Class H – Kerf width criteria	57
Figure 61 – Class H – Laser trim kerf extension into metallization criteria	57
Figure 62 – Class H – Resistor width reduction and untrimmed resistor material criteria	58
Figure 63 – Class H – Dielectric extension criteria	59
Figure 64 – Solder wetting criteria	60
Figure 65 – Solder wetting contact angle	60
Figure 66 – Element attachments	61
Figure 67 – Balling of die attach material	62
Figure 68 – Adhesive irregularities and cracks	63
Figure 69 – Adhesive string criterion	63
Figure 70 – Package post criteria	64
Figure 71 – Dual-in-line package leads solder wetting	65
Figure 72 – Lead to pad registration	66
Figure 73 – Lap joint solder wetting	67
Figure 74 – Combined butt and lap joints solder wetting – Reject	68
Figure 75 – Combined butt and lap joints solder wetting – Accept	69
Figure 76 – Solder fillet coverage criteria	69
Figure 77 – Acceptable symmetrical element orientation	71
Figure 78 – Bond dimensions	72
Figure 79 – Bond dimensions	73
Figure 80 – One bond used to secure two common wires	73
Figure 81 a) – Beam lead area and location	74
Figure 81 b) – Beam lead area and location	75
Figure 82 – Acceptable/rejectable tears or voids in ribbon weld area	75
Figure 83 – Criterion for strands along the mesh	76
Figure 84 – Criterion for continuous conducting paths	76
Figure 85 – Centre contact orientations to substrate	79
Figure 86 – Centre contact overlap to substrate	79
Figure 87 a) – Void criterion	80
Figure 87 b) – Crack/adhesion criteria	80

Figure 87 c) – Excess solder criterion	80
Figure 87 d) – Insufficient solder criterion	80
Figure 87 e) – Solder criteria.....	80
Figure 88 – Lead frame registration.....	81
Figure 89 – Dual-in-line lead frame registration.....	82
Figure 90 – Solder bridging	82
Figure 91 – Lead frame solder fillets	83
Figure 92 – Single finger solder fillet.....	83
Figure 93 – Substrate to lead frame fork gap.....	84
Figure 94 – Class H – Metallization protrusion criterion.....	84
Figure 95 – Class H – Metal plate exposure criteria	86
Figure 96 – Class H – Crack criteria.....	86
Figure 97 – Class H – Delamination criteria.....	86
Figure 98 – Class H – Termination non-conformance criteria.....	87
Figure 99 – Class H – Metallized edge non-conformance criteria.....	87
Figure 100 – Class H – Metallization extension criterion.....	88
Figure 101 – Class H – Crack in dielectric criterion	89
Figure 102 – Class H – Resistor width reduction criterion.....	90
Figure 103 – Class H – Termination width criterion	90
Figure 104 – Class H – Substrate non-conformance criteria.....	91
Figure 105 – Class H – Termination material build-up criteria.....	91
Figure 106 – Class H – Termination material splatter criteria.....	92
Table 1 – Shaker frequencies.....	97

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –**Part 23-2: Hybrid integrated circuits and film structures –
Manufacturing line certification –
Internal visual inspection and special tests**

FOREWORD

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International Standard IEC 60748-23-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-2 and the following documents:

FDIS	Report on voting
47A/639/FDIS	47A/650/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

IEC 60748-23-2 should be read in conjunction with Parts 23-1, 23-3 and 23-4.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This set of specifications prescribes a set of procedures to be used by users and manufacturers for the production and delivery of high-quality, special requirement hybrid integrated circuits and film structures with a specified level of quality and reliability.

This set of specifications prescribes reference criteria for the establishment, control, maintenance and development of a certified manufacturing line and represents a manufacturing line certification methodology.

The targeted level of quality and reliability is to be achieved by using best design and manufacturing practices. Examples of quality and reliability best practices for elimination of potential failure mechanisms and achievement of a targeted quality and reliability level include: material characterization for derivation of process design rules, in-process control, continuous improvement, etc.

Assessment (estimation) of the targeted quality and reliability level may be accomplished by:

- a) using data obtained from the material characterization, design and process control and improvement activities; or
- b) through the use of product assessment level schedule (PALS) tests.

Part 23-1 of this set of specifications provides general information.

Part 23-3 of this set of specifications provides a framework for use as an assessment/audit tool to assist the suppliers, customers or an independent organization to carry out an assessment of a certified manufacturing line of a hybrid manufacturing company.

Part 23-4 of this set of specifications provides a blank detail specification, which provides guidance to 'users' of hybrids for procurement purposes.

Part 23-5 of this set of specifications provides a means of quality assessment on the basis of qualification approval.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

1 Scope

This part of IEC 60748 applies to high quality approval systems for hybrid integrated circuits and film structures.

The purpose of the tests is to perform visual inspections on the internal materials, construction and workmanship of hybrid, multichip and multichip module microcircuits and passive elements used for microelectronic applications including r.f./microwave.

These tests are for both Class H and Class K quality levels, SAW and film hybrid/multichip/multichip module microcircuits using substrates such as ceramic and silicon. Class K is applicable to all microcircuits released to product assessment level schedule 11 (e.g. for space applications – see IEC 60748-23-1). Class H is applicable to all other microcircuits released to this standard. The following types of microcircuits may be inspected:

- a) passive thin and thick film networks;
- b) active thin and thick film circuits;
- c) multiple circuits, including combinations, stacking or other interconnections of 1 a) and 1 b).

Where the deposited film has geometric features larger than 25 µm, the inspection criteria defined in clause 5 apply. In cases where deposited features are smaller than this (e.g. deposited integrated circuits) the inspection requirements of IEC 60747 shall be applied.

These tests will normally be used on microelectronic devices prior to capping or encapsulation to detect and eliminate devices with internal non-conformances that could lead to device failure in normal application. They may also be employed on a sampling basis to determine the effectiveness of the manufacturers' quality control and handling procedures.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary*

IEC 60747-1:1983, *Semiconductor devices – Discrete devices – Part 1: General*¹

Amendment 3 (1996)

IEC 60748-1, *Semiconductor devices – Integrated circuits – Part 1: General*¹

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

¹ Together with any other part of IEC 60747 or IEC 60748 relevant to the specific hybrid application, including terminology.

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Manufacturers' self-audit checklist and report*

IEC 60748-23-4:2002, *Semiconductor devices – Integrated circuits – Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification*

IEC 61191-2:1998, *Printed board assemblies – Part 2: Sectional specification – Requirements for surface mount soldered assemblies*

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

EN 100012:1995, *Basic Specification: X-ray inspection of electronic components*

3 Definitions

For the purpose of this part of IEC 60748, the definitions given in IEC 60050, IEC 60747, IEC 60748-1 and IEC 60748-23-1, as well as the following definitions, shall apply.

3.1

active circuit area

includes all areas of functional circuit elements, operating metallization or connected combinations thereof excluding beam leads; in the case of resistors, includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads)

3.2

add-on substrate

supporting structural material into and/or upon which glassivation, metallization and circuit elements are placed and the entire assembly is in turn placed on and attached to the main substrate

3.3

attachment medium

material used to effect the attachment of an element to an underlying surface (e.g. adhesive, solder, alloy)

3.4

blister, metallization

hollow bump that can be flattened

3.5

block resistor

solid, rectangularly shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements

3.6

bonding pad

metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element

3.7

bonding site

metallized area on a substrate or element intended for a wire or ribbon interconnecting bond

3.8

bridging

complete connection between circuit features not intended to be connected

3.9

cold solder joint

solder joint whose appearance is "grainy" or "dull"

NOTE Where a "grainy" or "dull" appearance is characteristic of certain solder materials (e.g. AuSn, etc.), this criterion should not cause these materials to be rejected.

3.10

compound bond

one bond on top of another

3.11

conductive attach

process and materials used for the attachment that also provides an electrical contact or thermal dissipation path (e.g. solder, eutectic, solder-impregnated epoxy)

3.12

conductive substrate

substrate that can conduct electricity

NOTE Copper or doped silicon, for example, are conductive substrates while alumina and quartz are non-conductive (insulating) substrates.

3.13

contact window

opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate

3.14

controlled environment

environment that is in accordance with the requirements of the appropriate product assessment level schedules (PALS) in Annex A of IEC 60748-23-1 and with respect to cleanroom class and (where specified) temperature and relative humidity

3.15

corrosion

gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product

3.16

coupling (air) bridge

raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material

3.17

crazing

presence of numerous, minute, interconnected surface cracks

3.18

crossover

transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing

3.19

detritus

fragments of original or trim-modified resistor or conductor material

3.20

dielectric

insulating material that does not conduct electricity but may be able to sustain an electric field

NOTE It can be used in crossovers, as a passivation or a glassivation, or in capacitors.

3.21**dielectric attach**

process and materials used for attachment that does not provide electrical contact or thermal dissipation

3.22**edge metallization**

metallization that electrically connects the metallization from the top surface to the opposite side of the substrate

3.23**element**

constituent of a hybrid microcircuit; such as integral deposited or screened passive elements, substrates, discrete or integrated electronic parts including dies, chips and other microcomponents; also mechanical piece parts such as cases and covers; all contributing to the operation of a hybrid microcircuit

3.24**electrically common**

satisfied when two or more conductive surfaces or interconnects are of equal d.c. voltage/signal potential

3.25**end terminated or wrap-around elements**

those elements which have electrical connections on the ends (sides) and/or base of their bodies

3.26**foreign material**

any material that is foreign to the element or microcircuit or any non-foreign material that is displaced from its original or intended position in the element or microcircuit package

NOTE It is considered attached when it cannot be removed by a nominal gas blow (approximately 138 kN/m²) (20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of colour fringing around the periphery of the particle.

3.27**glassivation**

top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads

NOTE Craze is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.

3.28**insulating layer**

dielectric layer used to isolate single or multilevel conductive and resistive material or to protect top level conductive resistive material

3.29**intermetallics (purple plague)**

one of several gold-aluminium compounds formed when bonding gold to aluminium and activated by re-exposure to moisture and high temperature (> 340 °C)

NOTE Purple plague is purplish in colour and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.