
**Vmesniki univerzalnega serijskega vodila za prenos podatkov in napajanje - 2-1.
del: Specifikacija univerzalnega serijskega vodila, revizija 2.0 (TA 14) (IEC 62680-2-1:2015)**

Universal Serial Bus interfaces for data and power - Part 2-1: Universal Serial Bus Specification, Revision 2.0 (TA 14) (IEC 62680-2-1:2015)

Schnittstellen des Universellen Seriellen Busses für Daten und Energie - Teil 2-1: Festlegung des Universellen Seriellen Busses, Überarbeitung 2.0 (IEC 62680-2-1:2015)
(standards.iteh.ai)

Interfaces de bus universel en série pour les données et l'alimentation électrique - Partie 2-1 : spécification du bus universel en série, révision 2.0 (TA 14) (IEC 62680-2-1:2015)

Ta slovenski standard je istoveten z: EN 62680-2-1:2015

ICS:

35.200	Vmesniška in povezovalna oprema	Interface and interconnection equipment
--------	---------------------------------	---

SIST EN 62680-2-1:2016

en,fr,de

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN 62680-2-1:2016

<https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-23485540b7f9/sist-en-62680-2-1-2016>

EUROPEAN STANDARD

EN 62680-2-1

NORME EUROPÉENNE

EUROPÄISCHE NORM

December 2015

ICS 29.220; 33.120; 35.200

English Version

Universal Serial Bus interfaces for data and power - Part 2-1:
Universal Serial Bus Specification, Revision 2.0 (TA 14)
(IEC 62680-2-1:2015)

Interfaces de bus universel en série pour les données et
l'alimentation électrique - Partie 2-1 : spécification du bus
universel en série, révision 2.0 (TA 14)
(IEC 62680-2-1:2015)

Schnittstellen des Universellen Seriellen Busses für Daten
und Energie - Teil 2-1: Festlegung des Universellen
Seriellen Busses, Überarbeitung 2.0
(IEC 62680-2-1:2015)

This European Standard was approved by CENELEC on 2015-10-20. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

SIST EN 62680-2-1:2016

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.



European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

EN 62680-2-1:2015**European foreword**

The text of document 100/2331/CDV, future edition 1 of IEC 62680-2-1, prepared by Technical Area 14 "Interfaces and methods of measurement for personal computing equipment" of IEC/TC 100 "Audio, video and multimedia systems and equipment" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62680-2-1:2015.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2016-07-20
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2018-10-20

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62680-2-1:2015 was approved by CENELEC as a European Standard without any modification.

ITEH STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 62680-2-1:2016](https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-23485540b7f9/sist-en-62680-2-1-2016)

<https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-23485540b7f9/sist-en-62680-2-1-2016>



INTERNATIONAL STANDARD



**Universal serial bus interfaces for data and power –
Part 2-1: Universal Serial Bus Specification, Revision 2.0**

STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 62680-2-1:2016](https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-23485540b7f9/sist-en-62680-2-1-2016)

<https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-23485540b7f9/sist-en-62680-2-1-2016>

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 29.220; 33.120; 35.200

ISBN 978-2-8322-2845-6

Warning! Make sure that you obtained this publication from an authorized distributor.

INTERNATIONAL ELECTROTECHNICAL COMMISSION

UNIVERSAL SERIAL BUS INTERFACES FOR DATA AND POWER –

Part 2-1: Universal Serial Bus Specification, Revision 2.0

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
<http://standards.iteh.ai/catalog/standards/sist/085754fd-4bb-4111-8720-208544000000/iec-62680-2-1-2015>
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62680-2-1 has been prepared by technical area 14: Interfaces and methods of measurement for personal computing equipment, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard is based on documents prepared by the USB Implementers Forum (USB-IF). The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

The text of this standard is based on the following documents:

CDV	Report on voting
100/2331/CDV	100/2434/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of all the parts in the IEC 62680 series, published under the general title *Universal serial bus interfaces for data and power* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

ITEH STANDARD PREVIEW
(standards.iteh.ai)

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

<https://standards.iteh.ai/catalog/standards/sist-en-62680-2-1-2016>
23485540b7f9/sist-en-62680-2-1-2016

INTRODUCTION

The IEC 62680 series is based on a series of specifications that were originally developed by the USB Implementers Forum (USB-IF). These specifications were submitted to the IEC under the auspices of a special agreement between the IEC and the USB IF.

The USB Implementers Forum, Inc.(USB-IF) is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. The Forum facilitates the development of high-quality compatible USB peripherals (devices), and promotes the benefits of USB and the quality of products that have passed compliance testing.

ANY USB SPECIFICATIONS ARE PROVIDED TO YOU "AS IS, "WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE USB IMPLEMENTERS FORUM AND THE AUTHORS OF ANY USB SPECIFICATIONS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OR INFORMATION IN THIS SPECIFICATION.

THE PROVISION OF ANY USB SPECIFICATIONS TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

Entering into USB Adopters' Agreements may, however, allow a signing company to participate in a reciprocal, royalty-free licensing arrangement for compliant products. For more information, please see:

<http://www.usb.org/developers/docs/>

http://www.usb.org/developers/devclass_docs#approved6

<https://standards.iteh.ai/catalog/standards/sist/08f754fd-c4bb-4111-8720-39130b8a5810/iec-62680-2-1-2015>

IEC DOES NOT TAKE ANY POSITION AS TO WHETHER IT IS ADVISABLE FOR YOU TO ENTER INTO ANY USB ADOPTERS AGREEMENTS OR TO PARTICIPATE IN THE USB IMPLEMENTERS FORUM.”

This series covers the Universal Series Bus interfaces for data and power and consists of the following parts:

IEC 62680-1-1, *Universal Serial Bus interfaces for data and power – Part 1-1: Common components – USB Battery Charging Specification, Revision 1.2*

IEC 62680-2-1, *Universal Serial Bus interfaces for data and power – Part 2-1: Universal Serial Bus Specification, Revision 2.0*

IEC 62680-2-2, *Universal Serial Bus interfaces for data and power – Part 2-2: USB Micro-USB Cables and Connectors Specification, Revision 1.01*

IEC 62680-2-3, *Universal Serial Bus interfaces for data and power – Part 2-3: Universal Serial Bus Cables and Connectors Class Document, Revision 2.0*

This part of the IEC 62680 series consists of several distinct parts:

- the main body of the text, which consists of the original specification and all ECN and Errata developed by the USB-IF.

CONTENTS

FOREWORD.....	2
INTRODUCTION.....	4
1 Chapter 1 Introduction.....	29
1.1 Motivation.....	29
1.2 Objective of the Specification.....	29
1.3 Scope of the Document.....	30
1.4 USB Product Compliance.....	30
1.5 Document Organization.....	30
2 Chapter 2 Terms and Abbreviations.....	31
3 Chapter 3 Background.....	37
3.1 Goals for the Universal Serial Bus.....	37
3.2 Taxonomy of Application Space.....	37
3.3 Feature List.....	38
4 Chapter 4 Architectural Overview.....	40
4.1 USB System Description.....	40
4.1.1 Bus Topology.....	40
4.2 Physical Interface.....	41
4.2.1 Electrical.....	42
4.2.2 Mechanical.....	42
4.3 Power.....	42
4.3.1 Power Distribution.....	43
4.3.2 Power Management.....	43
4.4 Bus Protocol.....	43
4.5 Robustness.....	43
4.5.1 Error Detection.....	44
4.5.2 Error Handling.....	44
4.6 System Configuration.....	44
4.6.1 Attachment of USB Devices.....	44
4.6.2 Removal of USB Devices.....	44
4.6.3 Bus Enumeration.....	45
4.7 Data Flow Types.....	45
4.7.1 Control Transfers.....	45
4.7.2 Bulk Transfers.....	45
4.7.3 Interrupt Transfers.....	45
4.7.4 Isochronous Transfers.....	46
4.7.5 Allocating USB Bandwidth.....	46
4.8 USB Devices.....	46
4.8.1 Device Characterizations.....	46
4.8.2 Device Descriptions.....	47
4.9 USB Host: Hardware and Software.....	49
4.10 Architectural Extensions.....	49
5 Chapter 5 USB Data Flow Model.....	50
5.1 Implementer Viewpoints.....	50
5.2 Bus Topology.....	51
5.2.1 USB Host.....	52
5.2.2 USB Devices.....	52

5.2.3	Physical Bus Topology	53
5.2.4	Logical Bus Topology	54
5.2.5	Client Software-to-function Relationship	55
5.3	USB Communication Flow.....	55
5.3.1	Device Endpoints.....	57
5.3.2	Pipes	58
5.3.3	Frames and Microframes	60
5.4	Transfer Types.....	60
5.4.1	Table Calculation Examples.....	61
5.5	Control Transfers	62
5.5.1	Control Transfer Data Format	62
5.5.2	Control Transfer Direction.....	63
5.5.3	Control Transfer Packet Size Constraints	63
5.5.4	Control Transfer Bus Access Constraints.....	64
5.5.5	Control Transfer Data Sequences	66
5.6	Isochronous Transfers	67
5.6.1	Isochronous Transfer Data Format.....	67
5.6.2	Isochronous Transfer Direction	67
5.6.3	Isochronous Transfer Packet Size Constraints	67
5.6.4	Isochronous Transfer Bus Access Constraints	69
5.6.5	Isochronous Transfer Data Sequences	70
5.7	Interrupt Transfers	70
5.7.1	Interrupt Transfer Data Format	70
5.7.2	Interrupt Transfer Direction.....	70
5.7.3	Interrupt Transfer Packet Size Constraints	70
5.7.4	Interrupt Transfer Bus Access Constraints	71
5.7.5	Interrupt Transfer Data Sequences	74
5.8	Bulk Transfers	74
5.8.1	Bulk Transfer Data Format.....	74
5.8.2	Bulk Transfer Direction	74
5.8.3	Bulk Transfer Packet Size Constraints	74
5.8.4	Bulk Transfer Bus Access Constraints	75
5.8.5	Bulk Transfer Data Sequences	76
5.9	High-Speed, High Bandwidth Endpoints	77
5.9.1	High Bandwidth Interrupt Endpoints.....	77
5.9.2	High Bandwidth Isochronous Endpoints	78
5.10	Split Transactions	79
5.11	Bus Access for Transfers	79
5.11.1	Transfer Management.....	80
5.11.2	Transaction Tracking	82
5.11.3	Calculating Bus Transaction Times	84
5.11.4	Calculating Buffer Sizes in Functions and Software	86
5.11.5	Bus Bandwidth Reclamation	86
5.12	Special Considerations for Isochronous Transfers.....	86
5.12.1	Example Non-USB Isochronous Application.....	88
5.12.2	USB Clock Model.....	89
5.12.3	Clock Synchronization	91
5.12.4	Isochronous Devices	91
5.12.5	Data Prebuffering	99

5.12.6	SOF Tracking	100
5.12.7	Error Handling	100
5.12.8	Buffering for Rate Matching	101
6	Chapter 6 Mechanical	103
6.1	Architectural Overview	103
6.2	Keyed Connector Protocol	103
6.3	Cable	104
6.4	Cable Assembly	104
6.4.1	Standard Detachable Cable Assemblies	104
6.4.2	High-/full-speed Captive Cable Assemblies	106
6.4.3	Low-speed Captive Cable Assemblies	108
6.4.4	Prohibited Cable Assemblies	110
6.5	Connector Mechanical Configuration and Material Requirements	110
6.5.1	USB Icon Location	111
6.5.2	USB Connector Termination Data	111
6.5.3	Series “A” and Series “B” Receptacles	112
6.5.4	Series “A” and Series “B” Plugs	115
6.6	Cable Mechanical Configuration and Material Requirements	118
6.6.1	Description	119
6.6.2	Construction	119
6.6.3	Electrical Characteristics	122
6.6.4	Cable Environmental Characteristics	122
6.6.5	Listing	122
6.7	Electrical, Mechanical, and Environmental Compliance Standards	123
6.7.1	Applicable Documents	128
6.8	USB Grounding	128
6.9	PCB Reference Drawings	128
7	Chapter 7 Electrical	132
7.1	Signaling	132
7.1.1	USB Driver Characteristics	135
7.1.2	Data Signal Rise and Fall, Eye Patterns	142
7.1.3	Cable Skew	151
7.1.4	Receiver Characteristics	151
7.1.5	Device Speed Identification	153
7.1.6	Input Characteristics	154
7.1.7	Signaling Levels	157
7.1.8	Data Encoding/Decoding	170
7.1.9	Bit Stuffing	170
7.1.10	Sync Pattern	172
7.1.11	Data Signaling Rate	173
7.1.12	Frame Interval	173
7.1.13	Data Source Signaling	174
7.1.14	Hub Signaling Timings	175
7.1.15	Receiver Data Jitter	177
7.1.16	Cable Delay	179
7.1.17	Cable Attenuation	180
7.1.18	Bus Turn-around Time and Inter-packet Delay	181
7.1.19	Maximum End-to-end Signal Delay	182
7.1.20	Test Mode Support	183

7.2	Power Distribution.....	184
7.2.1	Classes of Devices	184
7.2.2	Voltage Drop Budget	189
7.2.3	Power Control During Suspend/Resume	189
7.2.4	Dynamic Attach and Detach.....	190
7.3	Physical Layer	191
7.3.1	Regulatory Requirements	191
7.3.2	Bus Timing/Electrical Characteristics.....	192
7.3.3	Timing Waveforms	202
8	Chapter 8 Protocol Layer.....	205
8.1	Byte/Bit Ordering	205
8.2	SYNC Field.....	205
8.3	Packet Field Formats	205
8.3.1	Packet Identifier Field.....	205
8.3.2	Address Fields.....	206
8.3.3	Frame Number Field	207
8.3.4	Data Field.....	207
8.3.5	Cyclic Redundancy Checks.....	208
8.4	Packet Formats.....	209
8.4.1	Token Packets.....	209
8.4.2	Split Transaction Special Token Packets.....	209
8.4.3	Start-of-Frame Packets.....	214
8.4.4	Data Packets.....	215
8.4.5	Handshake Packets.....	216
8.4.6	Handshake Responses.....	217
8.5	Transaction Packet Sequences.....	218
8.5.1	NAK Limiting via Ping Flow Control.....	227
8.5.2	Bulk Transactions	231
8.5.3	Control Transfers.....	236
8.5.4	Interrupt Transactions.....	239
8.5.5	Isochronous Transactions.....	239
8.6	Data Toggle Synchronization and Retry	243
8.6.1	Initialization via SETUP Token.....	244
8.6.2	Successful Data Transactions.....	244
8.6.3	Data Corrupted or Not Accepted	245
8.6.4	Corrupted ACK Handshake.....	245
8.6.5	Low-speed Transactions	246
8.7	Error Detection and Recovery	247
8.7.1	Packet Error Categories	247
8.7.2	Bus Turn-around Timing	247
8.7.3	False EOPs	248
8.7.4	Babble and Loss of Activity Recovery	249
9	Chapter 9 USB Device Framework.....	250
9.1	USB Device States	250
9.1.1	Visible Device States.....	250
9.1.2	Bus Enumeration	254
9.2	Generic USB Device Operations	254
9.2.1	Dynamic Attachment and Removal	255
9.2.2	Address Assignment.....	255

9.2.3	Configuration	255
9.2.4	Data Transfer	256
9.2.5	Power Management	256
9.2.6	Request Processing	256
9.2.7	Request Error	258
9.3	USB Device Requests	259
9.3.1	bmRequestType	259
9.3.2	bRequest	259
9.3.3	wValue	259
9.3.4	wIndex	260
9.3.5	wLength	260
9.4	Standard Device Requests	260
9.4.1	Clear Feature	262
9.4.2	Get Configuration	263
9.4.3	Get Descriptor	263
9.4.4	Get Interface	264
9.4.5	Get Status	264
9.4.6	Set Address	266
9.4.7	Set Configuration	266
9.4.8	Set Descriptor	267
9.4.9	Set Feature	268
9.4.10	Set Interface	269
9.4.11	Synch Frame	269
9.5	Descriptors	270
9.6	Standard USB Descriptor Definitions	270
9.6.1	Device	270
9.6.2	Device_Qualifier	272
9.6.3	Configuration	273
9.6.4	Other_Speed_Configuration	275
9.6.5	Interface	275
9.6.6	Endpoint	276
9.6.7	String	279
9.7	Device Class Definitions	280
9.7.1	Descriptors	280
9.7.2	Interface(s) and Endpoint Usage	280
9.7.3	Requests	281
10	Chapter 10 USB Host: Hardware and Software	282
10.1	Overview of the USB Host	282
10.1.1	Overview	282
10.1.2	Control Mechanisms	285
10.1.3	Data Flow	285
10.1.4	Collecting Status and Activity Statistics	286
10.1.5	Electrical Interface Considerations	286
10.2	Host Controller Requirements	286
10.2.1	State Handling	287
10.2.2	Serializer/Deserializer	287
10.2.3	Frame and Microframe Generation	287
10.2.4	Data Processing	288
10.2.5	Protocol Engine	288

10.2.6	Transmission Error Handling.....	288
10.2.7	Remote Wakeup	289
10.2.8	Root Hub	289
10.2.9	Host System Interface	289
10.3	Overview of Software Mechanisms.....	289
10.3.1	Device Configuration	290
10.3.2	Resource Management.....	292
10.3.3	Data Transfers.....	292
10.3.4	Common Data Definitions	293
10.4	Host Controller Driver	293
10.5	Universal Serial Bus Driver	294
10.5.1	USB D Overview.....	294
10.5.2	USB D Command Mechanism Requirements	296
10.5.3	USB D Pipe Mechanisms.....	298
10.5.4	Managing the USB via the USB D Mechanisms.....	300
10.5.5	Passing USB Preboot Control to the Operating System	302
10.6	Operating System Environment Guides.....	302
11	Chapter 11 Hub Specification	303
11.1	Overview	303
11.1.1	Hub Architecture.....	303
11.1.2	Hub Connectivity.....	304
11.2	Hub Frame/Microframe Timer.....	306
11.2.1	High-speed Microframe Timer Range.....	306
11.2.2	Full-speed Frame Timer Range.....	306
11.2.3	Frame/Microframe Timer Synchronization.....	307
11.2.4	Microframe Jitter Related to Frame Jitter.....	309
11.2.5	EOF1 and EOF2 Timing Points.....	309
11.3	Host Behavior at End-of-Frame.....	312
11.3.1	Full-/low-speed Latest Host Packet.....	312
11.3.2	Full-/low-speed Packet Nullification	312
11.3.3	Full-/low-speed Transaction Completion Prediction.....	313
11.4	Internal Port.....	313
11.4.1	Inactive.....	314
11.4.2	Suspend Delay	314
11.4.3	Full Suspend (Fsus)	314
11.4.4	Generate Resume (GResume).....	314
11.5	Downstream Facing Ports	315
11.5.1	Downstream Facing Port State Descriptions	317
11.5.2	Disconnect Detect Timer.....	321
11.5.3	Port Indicator.....	322
11.6	Upstream Facing Port.....	324
11.6.1	Full-speed	324
11.6.2	High-speed	325
11.6.3	Receiver	325
11.6.4	Transmitter	328
11.7	Hub Repeater	330
11.7.1	High-speed Packet Connectivity	330
11.7.2	Hub Repeater State Machine.....	332
11.7.3	Wait for Start of Packet from Upstream Port (WFSOPFU).....	334

11.7.4	Wait for End of Packet from Upstream Port (WFEOPFU)	334
11.7.5	Wait for Start of Packet (WFSOP)	334
11.7.6	Wait for End of Packet (WFEO)	334
11.8	Bus State Evaluation	335
11.8.1	Port Error	335
11.8.2	Speed Detection	335
11.8.3	Collision	336
11.8.4	Low-speed Port Behavior	336
11.9	Suspend and Resume	337
11.10	Hub Reset Behavior	339
11.11	Hub Port Power Control	339
11.11.1	Multiple Gangs	340
11.12	Hub Controller	340
11.12.1	Endpoint Organization	341
11.12.2	Hub Information Architecture and Operation	341
11.12.3	Port Change Information Processing	342
11.12.4	Hub and Port Status Change Bitmap	343
11.12.5	Over-current Reporting and Recovery	344
11.12.6	Enumeration Handling	345
11.13	Hub Configuration	345
11.14	Transaction Translator	346
11.14.1	Overview	347
11.14.2	Transaction Translator Scheduling	349
11.15	Split Transaction Notation Information	351
11.16	Common Split Transaction State Machines	354
11.16.1	Host Controller State Machine	355
11.16.2	Transaction Translator State Machine	359
11.17	Bulk/Control Transaction Translation Overview	364
11.17.1	Bulk/Control Split Transaction Sequences	365
11.17.2	Bulk/Control Split Transaction State Machines	371
11.17.3	Bulk/Control Sequencing	376
11.17.4	Bulk/Control Buffering Requirements	377
11.17.5	Other Bulk/Control Details	377
11.18	Periodic Split Transaction Pipelining and Buffer Management	377
11.18.1	Best Case Full-Speed Budget	378
11.18.2	TT Microframe Pipeline	378
11.18.3	Generation of Full-speed Frames	379
11.18.4	Host Split Transaction Scheduling Requirements	379
11.18.5	TT Response Generation	382
11.18.6	TT Periodic Transaction Handling Requirements	383
11.18.7	TT Transaction Tracking	385
11.18.8	TT Complete-split Transaction State Searching	386
11.19	Approximate TT Buffer Space Required	387
11.20	Interrupt Transaction Translation Overview	387
11.20.1	Interrupt Split Transaction Sequences	388
11.20.2	Interrupt Split Transaction State Machines	391
11.20.3	Interrupt OUT Sequencing	397
11.20.4	Interrupt IN Sequencing	398
11.21	Isochronous Transaction Translation Overview	399