
**Road vehicles — Controller area
network (CAN) conformance test
plan —**

**Part 1:
Data link layer and physical signalling**

*Véhicules routiers — Plan d'essai de conformité du gestionnaire de
réseau de communication (CAN) —*

Partie 1: Couche liaison de données et signalisation physique

Document Preview

[ISO 16845-1:2016](https://standards.iteh.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016)

<https://standards.iteh.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016>



iTeh Standards
(<https://standards.iteh.ai>)
Document Preview

[ISO 16845-1:2016](https://standards.iteh.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016)

<https://standards.iteh.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016>



COPYRIGHT PROTECTED DOCUMENT

© ISO 2016, Published in Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized otherwise in any form or by any means, electronic or mechanical, including photocopying, or posting on the internet or an intranet, without prior written permission. Permission can be requested from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office
Ch. de Blandonnet 8 • CP 401
CH-1214 Vernier, Geneva, Switzerland
Tel. +41 22 749 01 11
Fax +41 22 749 09 47
copyright@iso.org
www.iso.org

Contents

	Page
Foreword	vii
Introduction	viii
1 Scope	1
2 Normative references	1
3 Terms and definitions	1
4 Abbreviated terms	3
5 Global overview	4
5.1 Scope of test plan.....	4
5.2 Architecture of test plan.....	4
5.3 Organization.....	5
5.3.1 General organization.....	5
5.3.2 Test case organization.....	6
5.3.3 Hierarchical structure of tests.....	7
6 LT parameters	8
6.1 Overview.....	8
6.2 Description of parameters.....	8
6.2.1 Communication parameters.....	8
6.2.2 Application parameters.....	9
6.2.3 Bit rate configuration parameter variation for bit timing tests.....	10
7 Test type 1, received frame	10
7.1 Test class 1, valid frame format.....	10
7.1.1 Identifier and number of data test in base format.....	10
7.1.2 Identifier and number of data test in extended format.....	11
7.1.3 Reception after arbitration lost.....	12
7.1.4 Acceptance of non-nominal bit in base format frame.....	13
7.1.5 Acceptance of non-nominal bit in extended format frame.....	13
7.1.6 Protocol exception behaviour on non-nominal bit.....	14
7.1.7 Minimum time for bus idle after protocol exception handling.....	15
7.1.8 DLC greater than 8.....	15
7.1.9 Absent bus idle — Valid frame reception.....	16
7.1.10 Stuff acceptance test in base format frame.....	16
7.1.11 Stuff acceptance test in extended format frame.....	17
7.1.12 Message validation.....	18
7.2 Test class 2, error detection.....	19
7.2.1 Bit error in data frame.....	19
7.2.2 Stuff error for basic frame.....	19
7.2.3 Stuff error for extended frame.....	20
7.2.4 Stuff error for FD frame payload bytes.....	21
7.2.5 CRC error.....	22
7.2.6 Combination of CRC error and form error.....	23
7.2.7 Form error in data frame at “CRC delimiter” bit position.....	24
7.2.8 Form error at fixed stuff bit in FD frames.....	24
7.2.9 Form error in data frame at “ACK delimiter” bit position.....	25
7.2.10 Form error in data frame at “EOF”.....	25
7.2.11 Message non-validation.....	26
7.3 Test class 3, error frame management.....	26
7.3.1 Error flag longer than 6 bits.....	26
7.3.2 Data frame starting on the third bit of intermission field.....	27
7.3.3 Bit error in error flag.....	27
7.3.4 Form error in error delimiter.....	28
7.4 Test class 4, overload frame management.....	28
7.4.1 MAC overload generation during intermission field.....	28

7.4.2	Last bit of EOF	29
7.4.3	Eighth bit of an error and overload delimiter	29
7.4.4	Bit error in overload flag	30
7.4.5	Form error in overload delimiter	30
7.4.6	MAC overload generation during intermission field following an error frame	31
7.4.7	MAC overload generation during intermission field following an overload frame	31
7.5	Test class 5, passive error state class	32
7.5.1	Passive error flag completion test 1	32
7.5.2	Data frame acceptance after passive error frame transmission	33
7.5.3	Acceptance of 7 consecutive dominant bits after passive error flag	33
7.5.4	Passive state unchanged on further errors	34
7.5.5	Passive error flag completion — Test case 2	34
7.5.6	Form error in passive error delimiter	35
7.5.7	Transition from active to passive ERROR FLAG	35
7.6	Test class 6, error counter management	36
7.6.1	REC increment on bit error in active error flag	36
7.6.2	REC increment on bit error in overload flag	37
7.6.3	REC increment when active error flag is longer than 13 bits	37
7.6.4	REC increment when overload flag is longer than 13 bits	38
7.6.5	REC increment on bit error in the ACK field	38
7.6.6	REC increment on form error in CRC delimiter	38
7.6.7	REC increment on form error in ACK delimiter	39
7.6.8	REC increment on form error in EOF field	39
7.6.9	REC increment on stuff error	40
7.6.10	REC increment on CRC error	41
7.6.11	REC increment on dominant bit after end of error flag	41
7.6.12	REC increment on form error in error delimiter	42
7.6.13	REC increment on form error in overload delimiter	42
7.6.14	REC decrement on valid frame reception	43
7.6.15	REC decrement on valid frame reception during passive state	43
7.6.16	REC non-increment on last bit of EOF field	44
7.6.17	REC non-increment on 13-bit length overload flag	44
7.6.18	REC non-increment on 13-bit length error flag	45
7.6.19	REC non-increment on last bit of error delimiter	45
7.6.20	REC non-increment on last bit of overload delimiter	46
7.6.21	REC non-decrement on transmission	46
7.6.22	REC increment on form error at fixed stuff bit in FD frames	47
7.6.23	REC non-increment on protocol exception in FD frames	47
7.7	Test class 7, bit timing Classical CAN frame format	48
7.7.1	Sample point test	48
7.7.2	Hard synchronization on SOF reception	49
7.7.3	Synchronization when $e > 0$ and $e \leq \text{SJW}(N)$	49
7.7.4	Synchronization when $e > 0$ and $e > \text{SJW}(N)$	50
7.7.5	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$	50
7.7.6	Synchronization when $e < 0$ and $ e > \text{SJW}(N)$	51
7.7.7	Glitch filtering test on positive phase error	51
7.7.8	Glitch filtering test on negative phase error	52
7.7.9	Glitch filtering test in idle state	53
7.7.10	Non-Synchronization after a dominant sampled bit	54
7.7.11	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$ at “ACK” bit position	55
7.8	Test class 8, bit timing CAN FD frame format	55
7.8.1	Sample point test	55
7.8.2	Hard synchronization on “res” bit	58
7.8.3	Synchronization when $e > 0$ and $e \leq \text{SJW}(D)$	59
7.8.4	Synchronization when $e > 0$ and $e > \text{SJW}(D)$	61
7.8.5	Synchronization when $e < 0$ and $ e \leq \text{SJW}$	63
7.8.6	Synchronization when $e < 0$ and $ e > \text{SJW}$	65

7.8.7	Glitch filtering test on positive phase error.....	67
7.8.8	Glitch filtering test on negative phase error.....	69
7.8.9	No synchronization after a dominant sampled bit.....	71
8	Test type 2, transmitted frame.....	73
8.1	Test class 1, valid frame format.....	73
8.1.1	Identifier and number of data bytes test in base format.....	73
8.1.2	Identifier and number of data bytes test in extended format.....	73
8.1.3	Arbitration in base format frame.....	74
8.1.4	Arbitration in extended format frame test.....	75
8.1.5	Message validation.....	76
8.1.6	Stuff bit generation capability in base format frame.....	76
8.1.7	Stuff bit generation capability in extended frame.....	77
8.1.8	Transmission on the third bit of intermission field after arbitration lost.....	78
8.2	Test class 2, error detection.....	79
8.2.1	Bit error test in base format frame.....	79
8.2.2	Bit error in extended format frame.....	80
8.2.3	Stuff error test in base format frame.....	81
8.2.4	Stuff error test in extended frame format.....	81
8.2.5	Form error test.....	82
8.2.6	Acknowledgement error.....	83
8.2.7	Form field tolerance test for FD frame format.....	84
8.2.8	Bit error at stuff bit position for FD frame payload bytes.....	84
8.3	Test class 3, error frame management.....	85
8.3.1	Error flag longer than 6 bit.....	85
8.3.2	Transmission on the third bit of intermission field after error frame.....	85
8.3.3	Bit error in error flag.....	86
8.3.4	Form error in error delimiter.....	86
8.4	Test class 4, overload frame management.....	87
8.4.1	MAC overload generation in intermission field.....	87
8.4.2	Eighth bit of an error and overload delimiter.....	88
8.4.3	Transmission on the third bit of intermission after overload frame.....	88
8.4.4	Bit error in overload flag.....	89
8.4.5	Form error in overload delimiter.....	89
8.5	Test class 5, passive error state and bus-off.....	90
8.5.1	Acceptance of active error flag overwriting passive error flag.....	90
8.5.2	Frame acceptance after passive error frame transmission.....	90
8.5.3	Acceptance of 7 consecutive dominant bits after passive error flag.....	91
8.5.4	Reception of a frame during suspend transmission.....	92
8.5.5	Transmission of a frame after suspend transmission — Test case 1.....	92
8.5.6	Transmission of a frame after suspend transmission — Test case 2.....	93
8.5.7	Transmission of a frame after suspend transmission — Test case 3.....	93
8.5.8	Transmission of a frame without suspend transmission.....	93
8.5.9	No transmission of a frame between the third bit of intermission field and eighth bit of suspend transmission.....	94
8.5.10	Bus-off state.....	94
8.5.11	Bus-off recovery.....	95
8.5.12	Completion condition for a passive error flag.....	96
8.5.13	Form error in passive error delimiter.....	96
8.5.14	Maximum recovery time after a corrupted frame.....	97
8.5.15	Transition from active to passive ERROR FLAG.....	97
8.6	Test class 6, error counter management.....	98
8.6.1	TEC increment on bit error during active error flag.....	98
8.6.2	TEC increment on bit error during overload flag.....	99
8.6.3	TEC increment when active error flag is followed by dominant bits.....	99
8.6.4	TEC increment when passive error flag is followed by dominant bits.....	100
8.6.5	TEC increment when overload flag is followed by dominant bits.....	100
8.6.6	TEC increment on bit error in data frame.....	101
8.6.7	TEC increment on form error in a frame.....	102

8.6.8	TEC increment on acknowledgement error.....	102
8.6.9	TEC increment on form error in error delimiter.....	103
8.6.10	TEC increment on form error in overload delimiter.....	103
8.6.11	TEC decrement on successful frame transmission for TEC < 128.....	104
8.6.12	TEC decrement on successful frame transmission for TEC > 127.....	104
8.6.13	TEC non-increment on 13-bit long overload flag.....	105
8.6.14	TEC non-increment on 13-bit long error flag.....	105
8.6.15	TEC non-increment on form error at last bit of overload delimiter.....	106
8.6.16	TEC non-increment on form error at last bit of error delimiter.....	106
8.6.17	TEC non-increment on acknowledgement error in passive state.....	107
8.6.18	TEC increment after acknowledgement error in passive state.....	107
8.6.19	TEC non-increment on stuff error during arbitration.....	108
8.6.20	TEC non-decrement on transmission while arbitration lost.....	108
8.6.21	TEC non-increment after arbitration lost and error.....	109
8.7	Test class 7, bit timing.....	109
8.7.1	Sample point test.....	109
8.7.2	Hard synchronization on SOF reception before sample point.....	110
8.7.3	Hard synchronization on SOF reception after sample point.....	111
8.7.4	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$	111
8.7.5	Synchronization for $e < 0$ and $ e > \text{SJW}(N)$	112
8.7.6	Glitch filtering test on negative phase error.....	113
8.7.7	Non-synchronization on dominant bit transmission.....	113
8.7.8	Synchronization before information processing time.....	114
8.7.9	Synchronization after sample point while sending a dominant bit.....	114
8.8	Test class 8, bit timing CAN FD frame format.....	115
8.8.1	Sample point test.....	115
8.8.2	Secondary sample point test.....	118
8.8.3	No synchronization within data phase bits when $e < 0$; $ e \leq \text{SJW}(D)$	121
8.8.4	Glitch filtering test on negative phase error within FD frame bits.....	123
8.8.5	No synchronization on dominant bit transmission in FD frames.....	124
9	Test type 3, bi-directional frame.....	125
9.1	Test class 1, valid frame format.....	125
9.2	Test class 2, error detection.....	125
9.3	Test class 3, active error frame management.....	125
9.4	Test class 4, overload frame management.....	125
9.5	Test class 5, passive-error state and bus-off.....	125
9.6	Test class 6, error counter management.....	126
9.6.1	REC unaffected when increasing TEC.....	126
9.6.2	TEC unaffected when increasing REC.....	126

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

This first edition of ISO 16845-1 cancels and replaces ISO 16845:2004, which has been technically revised.

A list of all parts in the ISO 16845 series can be found on the ISO website.

Introduction

ISO 16845 was first published in 2004 to provide the methodology and abstract test suite necessary for checking the conformance of any CAN implementation of the CAN specified in ISO 11898-1.

iTeh Standards
(<https://standards.itih.ai>)
Document Preview

[ISO 16845-1:2016](https://standards.itih.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016)

<https://standards.itih.ai/catalog/standards/iso/7397ecc0-f0ad-4d6f-9010-a337e2f04ce4/iso-16845-1-2016>

Road vehicles — Controller area network (CAN) conformance test plan —

Part 1: Data link layer and physical signalling

1 Scope

This document specifies the conformance test plan for the CAN data link layer and the physical signalling as standardized in ISO 11898-1. This includes the Classical CAN protocols as well as the CAN FD protocols.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 11898-1:2015, *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

ISO/IEC 9646-1, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 1: General concepts*

ISO/IEC 9646-2, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 2: Abstract Test Suite specification*

ISO/IEC 9646-4, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 4: Test realization*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 11898-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp/>

3.1

bit rate prescaler

BRP

minimum time quantum used for a TQ in CAN Bit time configuration

3.2

conformance testing

applying the *test plan* (3.17) to an IUT

3.3

default state

state of the IUT

Note 1 to entry: The default state is characterized by the default value presented in 5.3.2.5.

3.4 dominant
represents the logical 0

3.5 dominant state
CAN bus is in dominant state when at least one CAN node drives a dominant value on the line

3.6 elementary test
repetitions of the test case for several values of the parameter to test

3.7 end of frame
last field of a data or remote frame before the intermission field

3.8 idle state
CAN bus is in idle state when no frame is started after intermission field

3.9 lower tester
supervises the *test suite* ([3.18](#))

3.10 REC passive state
device is in the passive state because the value of the REC has reached the error passive limit

3.11 recessive
represents the logical 1

3.12 recessive state
CAN bus is in the recessive state when no CAN node drives a dominant value on the line

3.13 TEC passive state
device is in the passive state because the value of the TEC has reached the error passive limit

3.14 test case
each test case is defined by a specific number and a particular name in the *test suite* ([3.18](#))

3.15 test class
each *test type* ([3.19](#)) is divided in eight test classes

3.16 test frame
CAN frames containing the test pattern specified in this document

3.17 test plan
specific application of the «OSI conformance testing general concepts» standard

3.18 test suite
checks the behaviour of the IUT for particular parameters of ISO 11898-1

3.19**test type**

defines the direction of the *test frames* (3.16)

EXAMPLE Behaviour of the IUT if receiving and/or transmitting messages.

3.20**upper tester**

acts as a user of the IUT

4 Abbreviated terms

All abbreviated terms in this document are written in upper case letters.

CTRL	Control field of CAN frame + SRR/RTR + IDE bit
CBFF: CTRL	= RTR, IDE, FDF, DLC merged together as 7 bit hexadecimal value
FBFF: CTRL	= RRS, IDE, FDF, res, BRS, ESI, DLC merged together as 10 bit hexadecimal value
CEFF: CTRL	= SRR, IDE, RTR, FDF, r0, DLC merged together as 9 bit hexadecimal value
FEFF: CTRL	= SRR, IDE, RRS, FDF, res, BRS, ESI, DLC merged together as 11 bit hexadecimal value
IPT	information processing time
LT	lower tester
NTQ(D)	number of time quantum in data bit rate
NTQ(N)	number of time quantum in nominal bit rate
Phase_Seg1(D)	Phase Segment 1 (Phase_Seg1) for data phase bit rate
Phase_Seg1(N)	Phase Segment 1 (Phase_Seg1) for nominal bit rate
Phase_Seg2(D)	Phase Segment 2 (Phase_Seg2) for data phase bit rate
Phase_Seg2(N)	Phase Segment 2 (Phase_Seg2) for nominal bit rate
Prop_Seg(D)	propagation segment (Prop_Seg) for data phase bit rate
Prop_Seg(N)	propagation segment (Prop_Seg) for nominal bit rate
Sampling_Point(D)	Sync_Seg(D) + Prop_Seg(D) + Phase_Seg1(D)
Sampling_Point(N)	Sync_Seg(N) + Prop_Seg(N) + Phase_Seg1(N)
SJW(D)	synchronization jump width (SJW) for data phase bit rate
SJW(N)	synchronization jump width (SJW) for nominal bit rate
Sync_Seg(D)	synchronization segment (Sync_Seg) for data phase bit rate
Sync_Seg(N)	synchronization segment (Sync_Seg) for nominal bit rate
TP	test plan

TQ(D)	time quantum in data bit rate
TQ(N)	time quantum in nominal bit rate
UT	upper tester

5 Global overview

5.1 Scope of test plan

ISO 9646-1, ISO 9646-2 and ISO 9646-4 define the methodology and the abstract test suite necessary to check the conformance of any CAN implementation to ISO 11898-1. The architecture of the TP is as shown in [Figure 1](#).

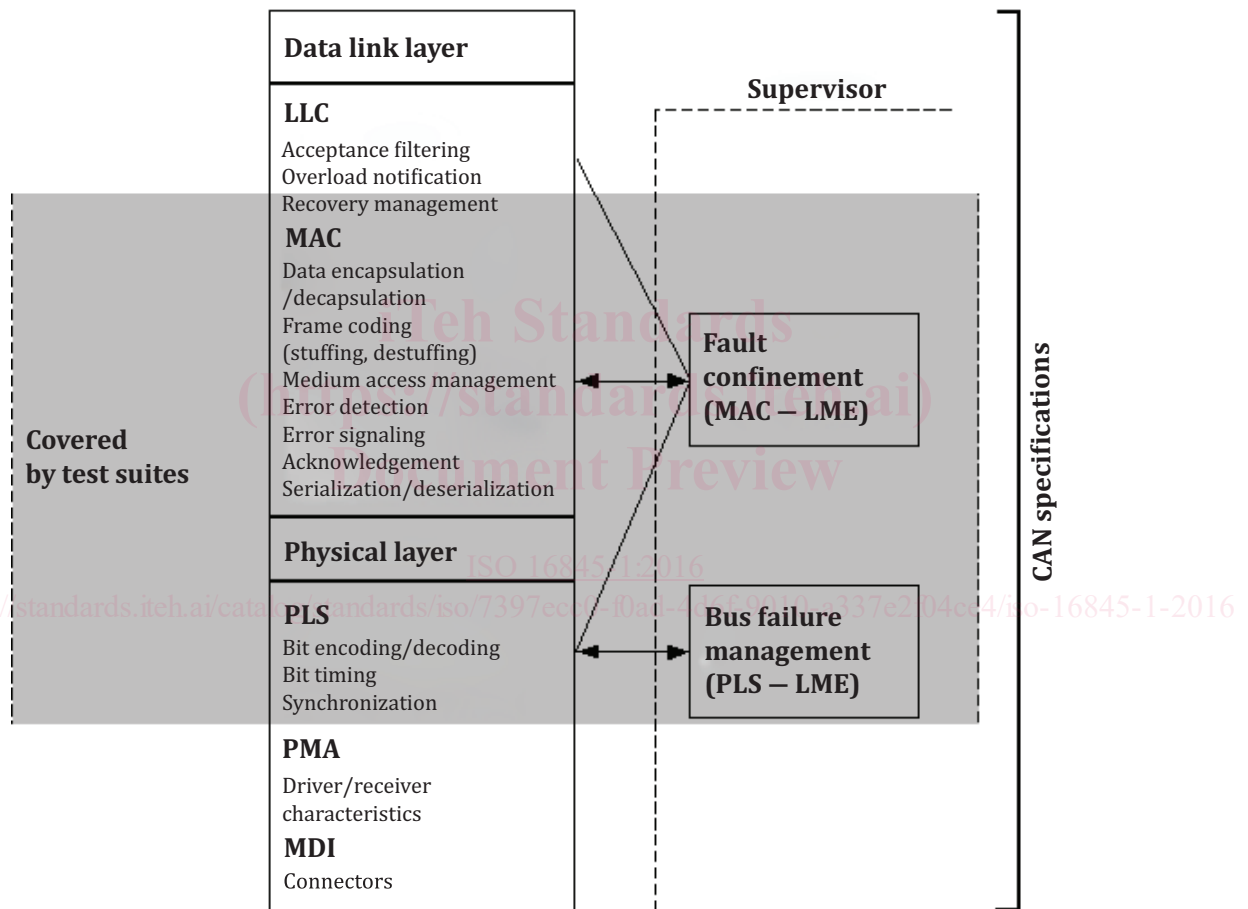


Figure 1 — Architecture of the test plan

5.2 Architecture of test plan

This methodology and the associated abstract test suites will be hereafter referred to as test plan (TP).

The TP is a specific application of the «OSI conformance testing general concepts» ISO 9646-1 and is restricted to the single party testing mode. Since the upper service boundary of a CAN implementation is not standardized and in some cases may not be observed and controlled [due to an application specific behaviour embedded in this implementation, for example, CAN SLIO (serial linked input/output)], the TP will rely either on the «coordinated test method» or the «remote test method».

Depending on the test method applied, the TP will involve up to the following three test functions:

- a lower tester (LT) operating in a way similar to the CAN implementation to be tested (IUT), running test suite and granting test verdict;
- an upper tester (UT) acting as user of the IUT (IUT dependant);
- a test management protocol between the IUT and the LT. The protocol consists in test coordination procedures.

The last two functions are only applicable to the coordinated test procedure.

During test execution, the LT can observe and control the standardized lower service boundary of the IUT (PCO) through the two service primitives provided by the CAN physical signalling sub-layer: PLS-Data.indicate and PLS-Data.request in most cases.

The environment that implements the TP is described in [Figure 2](#).

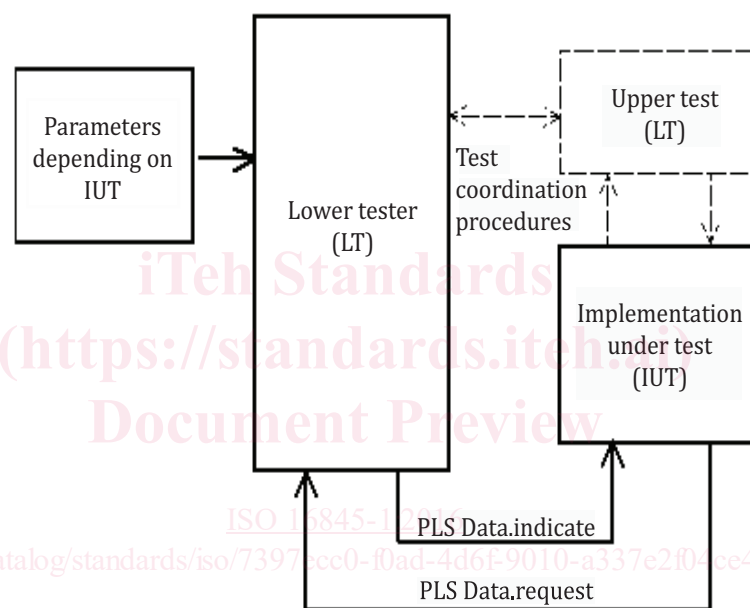


Figure 2 — CAN conformance TP environment

Using the network interface, the LT indicates to the UT the actions to be performed and the UT provides the LT with information concerning the internal behaviour of the IUT.

In order to allow the LT and the UT to communicate, it is necessary to define some test coordination procedures between them. These procedures use the network to the exclusion of any other physical link. They are used to set up the UT and to verify the test results.

5.3 Organization

5.3.1 General organization

The LT verifies if the IUT complies with the MAC, LLC and PLS sub-layers of ISO 11898-1. The LT points out differences between what is expected from the standard and the actual behaviour of the IUT.

The abstract test suites of the TP are independent to one another. Each abstract test suite checks the behaviour of the IUT for a particular parameter of ISO 11898-1. Each test case may be executed one after another in any order or alone.

Test cases requiring variations of individual parameters (identifier, number of data, etc.) should be repeated for each value of the parameter. Each repetition is named elementary test. A test case including different elementary tests is valid only if all tests pass.

5.3.2 Test case organization

5.3.2.1 General

Each elementary test is made of the following three states:

- set-up state;
- test state;
- verification state.

At the PCO, these states involve exchanges of valid sequences of PLS service primitives [CAN frame(s)] or invalid sequences of PLS primitives (invalid CAN frames or noise).

Before the first elementary test is started, the IUT has to be initialized into the default state.

5.3.2.2 Set-up state

The set-up state is the state in which the IUT has to be before entering the test state.

5.3.2.3 Test state

This is the part of the elementary test in which the parameter or protocol feature is actually checked. This state needs one or several exchanges or frames. These frames are named test frames.

5.3.2.4 Verification state

Verification state is made of the data reading frames which verify that the data have been handled in accordance with ISO 11898-1. These data should be checked.

For tests belonging to classes 1 to 6, the LT should be able to detect the correct value of the bit. For bit timing tests (classes 7 and 8), the LT should be able to detect a faulty synchronization of one time quantum.

For tests belonging to class 6, a readable error counter should be used for verification. In case the error counter value is not readable, the test should be applied by driving the IUT to the next error state by additional bus errors. The state change at expected position indicates the correct error counting up to this state change.

5.3.2.5 Default state

The default state is characterized by the following default value:

- both REC and TEC should be equal to 0;
- no pending transmission should be present;
- IUT should be in idle state;
- PLS-Data indicate and PLS-Data request should be recessive.

After the end of each elementary test, the default state should be applied.