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1 Scope

The present document describes the SPI interface for the communication of an SSP, as defined in ETSI TS 103 666-1 [1] using the SCL protocol.

2 References

2.1 Normative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

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The following referenced documents are necessary for the application of the present document.

[1] ETSI TS 103 666-1: "Smart Secure Platform (SSP); Part 1: General characteristics".

[2] ETSI TS 102 613: "Smart Cards; UICC - Contactless Front-end (CLF) Interface; Physical and data link layer characteristics".

[3] ISO/IEC 13239: "Information Technology -- Telecommunications and information exchange between systems -- High-level Data Link Control (HDLC) procedures".

2.2 Informative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

- In the case of a reference to a TC SCP document, a non-specific reference implicitly refers to the latest version of that document in the same Release as the present document.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

[i.1] ETSI TR 102 216: "Smart cards; Vocabulary for Smart Card Platform specifications".

3 Definition of terms, symbols and abbreviations

3.1 Terms

For the purposes of the present document, the terms given in ETSI TR 102 216 [i.1] and the following apply:

data transfer: information exchange during an SPI access between the master and the slave with SPI_MISO driven by the slave and SPI_MOSI driven by the master while the master is toggling the SPI_CLK signal

flow control: mechanism of the Data Link Layer that consists of methods applied by the transmitter in order to send at any time a number of logical data units that can be accepted by the receiver

frame: link layer data structure consisting of a prologue or frame header, payload and epilogue or trailer usually containing the CRC bytes

MAC access request: request from the slave to the master for a data transfer, i.e. a MAC phase initiated by the slave

MAC phase: initiation of a data transfer by the master and/or request for a data transfer by the slave

SPI access: SPI_NSS assertion by the master, if not already asserted in the MAC phase, followed by SPI_CLK start for transferring a certain number of bytes according to the SPI master configuration

NOTE: The number of bytes transferred during an SPI access is always the same in both directions on SPI_MISO and SPI_MOSI and is also referred to as access length.

window size: maximum number of logical data units that can be sent from the transmitter to the receiver without any link layer acknowledgements for any of these data units

window size slot: fixed space used by the slave in the receive buffer for the logical data units.

NOTE: The length of a window size slot equals the Data Link Layer MTU.

3.2 Symbols

Void.

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AC	Alternating Current
ACT	Activation
CLF	ContactLess Frontend
CMD	Command
CPHA	Clock Phase
CPOL	Clock Polarity
CRC	Cyclic Redundancy Check
DC	Direct Current
DLL	Data Link Layer
FIFO	First In, First Out
IO	Input/Output
IOH	High Output Current (Output current corresponding to VOH)
IOL	Low Output Current (Output current corresponding to VOL)
LLC	Logical Link Control
LPDU	Link Protocol Data Unit
MAC	Medium Access Control
MCT	MAC aCTivation
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MTU	Maximum Transmission Unit

NSD	Non-Significant Data
OD	Open Drain
RFU	Reserved for Future Use
SCL	SSP Common Layer
SHDLC	Simplified High Level Data Link Control
SPI	Serial Peripheral Interface
SSP	Smart Secure Platform
SWP	Single Wire Protocol

NOTE: Defined in ETSI TS 102 613 [2].

VDD	Supply Voltage
VIH	High Input Voltage (Input Voltage for High Logic Level)
VIL	Low Input Voltage (Input Voltage for Low Logic Level)
VOH	High Output Voltage (Output Voltage for High Logic Level)
VOL	Low Output Voltage (Output Voltage for Low Logic Level)

4 Introduction

The Serial Peripheral Interface (SPI) is a serial synchronous full-duplex communication interface between a single master and one or more slaves present on the same SPI bus, each slave being selected at one time by a dedicated SPI_NSS signal. This clause defines the physical, MAC and data link layers for the SPI interface.

In this clause the terms master and slave refer respectively to the terms master SPI and slave SPI.

5 SCL Under-Layers Protocol Stack

Figure 5.1 illustrates the protocol stack below the SCL supporting the SPI interface.

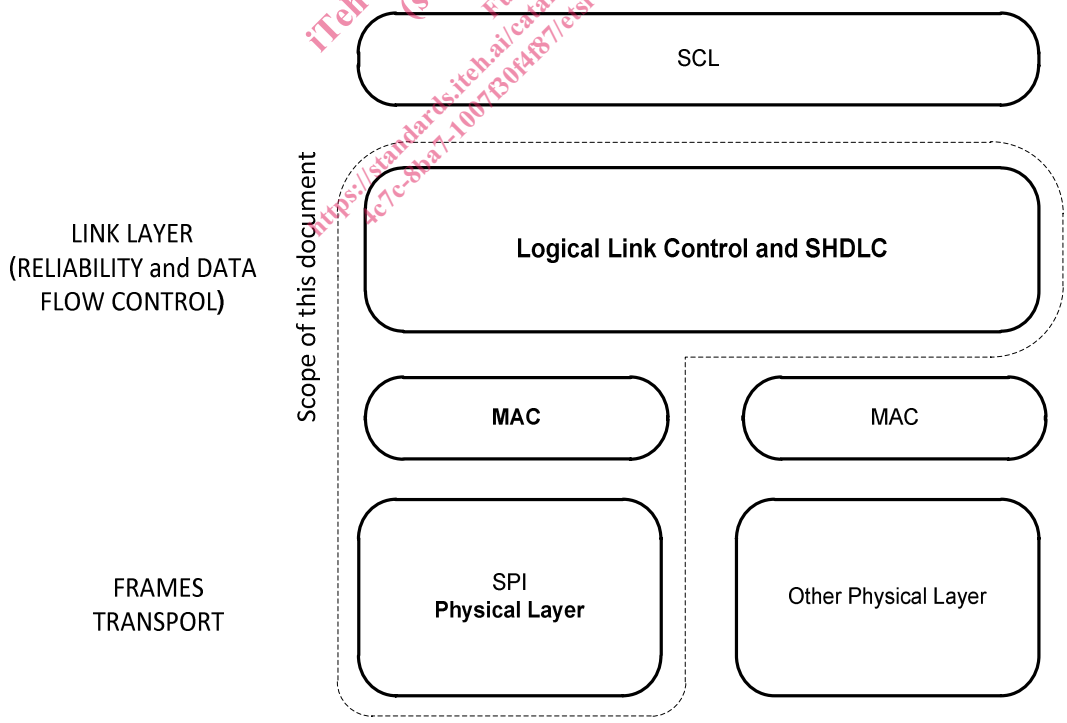

Figure 5.1: Protocol stack for SPI Interface

6 Electrical interfaces

6.1 Introduction

In the clauses below, different implementations of SPI interface are defined. These implementations allow bi-directional communication and the possibility for the slave to initiate communication with the master when it has data available thus avoiding the necessity for continuous polling to be performed by master.

Slave may initiate communication to send a command without a prior command from master.

6.2 Physical interface with 5 signals

Figure 6.1 illustrates the SPI electrical interface using 5 signals.

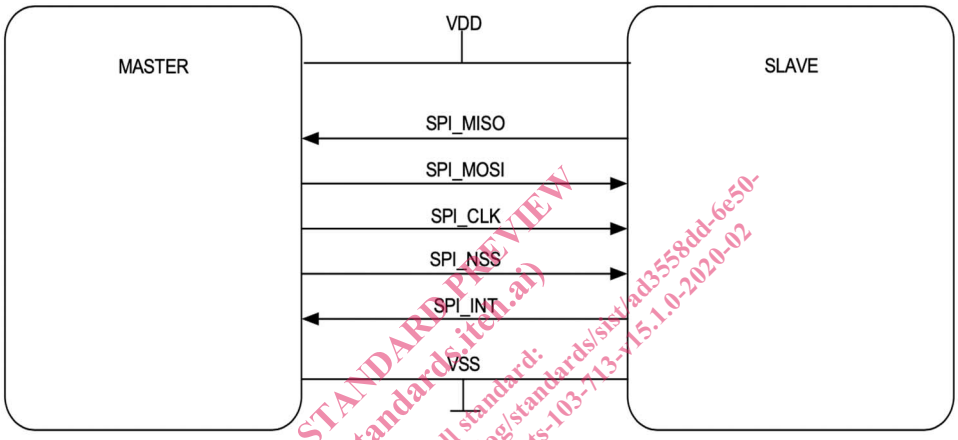

Figure 6.1: SPI electrical interface with 5 signals

This SPI interface describes two sets of signals:

- The generic and legacy SPI interface using the 4 signals: SPI_MOSI (Master Output Slave Input), SPI_MISO (Master Input Slave Output), SPI_CLK (clock) and the SPI_NSS signal used for the selection of a Slave Endpoint among N slaves sharing the same bus. SPI_MISO, SPI_MOSI and SPI_CLK can be shared between several SPI slaves present on the same SPI bus.
- The SPI_INT signal allows the slave to initiate a MAC access request in order to notify the master to start a data transfer.

SPI_INT signal is considered active or asserted at high voltage level.

SPI_NSS is considered active or asserted at low voltage level.

6.3 Physical interface with 4 signals

Figure 6.2 illustrates the SPI interface using 4 signals, bi-directional SPI_NSS.

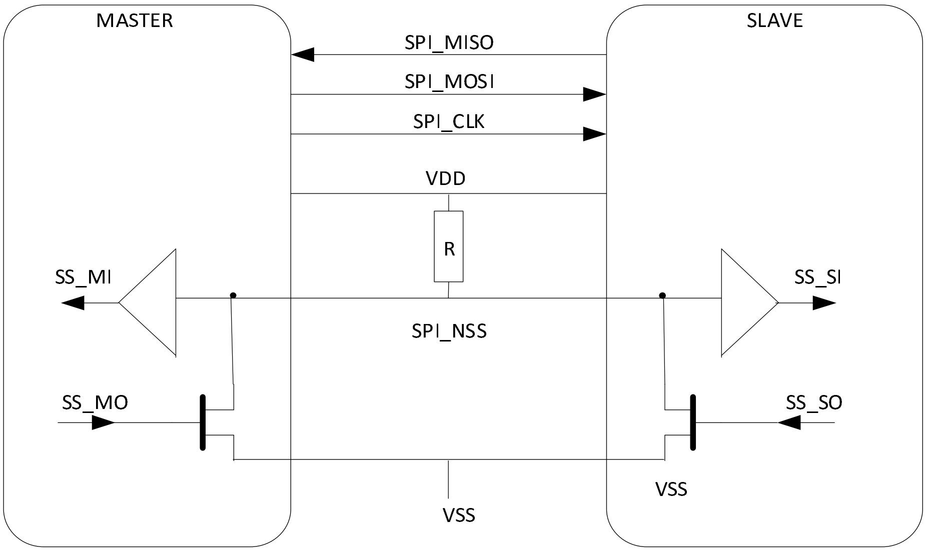

Figure 6.2: SPI electrical interface with 4 signals, bi-directional SPI_NSS

The SPI interface with 4 signals describes two sets of signals:

- The three generic and legacy SPI signals as SPI_MOSI (Master Output Slave Input), SPI_MISO (Master Input Slave Output) and SPI_CLK (clock). These signals can be shared between several SPI slaves as a bus.
- The SPI_NSS (Negative Slave Select) signal used for the selection of a slave endpoint among N slaves sharing the same bus and for the slave to initiate a MAC access request to notify the master to initiate a data transfer.

SPI_NSS is considered active or asserted at low voltage level. SPI_NSS requires a bidirectional IO implementing an Open Drain (OD) interface for both master and slave. This configuration allows driving the SPI_NSS signal to low voltage level by both master and slave without electrical contention.

A pull-up resistor allows to keep SPI_NSS at high state level (i.e. idle state) when SS_MO and SS_SO are not asserted. The SPI_NSS signal is at low state when either SS_MO or SS_SO are asserted.

NOTE: Despite the current industry de-facto SPI specification which defines SPI_NSS signal as unidirectional, driven by the master, in the present document the SPI_NSS in the 4 signals configuration is bidirectional.

Table 6.1: Definition of the signals

Signal	Description
SS_MO	Internal master output signal for SPI_NSS assertion. SS_MO is at high state level for generating a SPI_NSS signal assertion (i.e. low level state)
SS_SO	Internal slave output signal for SPI_NSS assertion. SS_SO is at high state level for generating a SPI_NSS signal assertion (i.e. low level state)
SS_MI	Internal master input signal indicating SPI_NSS status. SS_MI is at high state level when the SPI_NSS signal is not asserted
SS_SI	Internal slave input signal indicating SPI_NSS status. SS_SI is at high state level when the SPI_NSS signal is not asserted
SPI_NSS	SPI_NSS signal: low state level when asserted

6.4 Electrical characteristics

6.4.1 DC characteristics

The SPI Electrical specification interface shall be defined for VDD operational voltage classes B and C as defined in ETSI TS 103 666-1 [1], clause 6.2.2.3.

Table 6.2: DC characteristics for operational voltage class B

Parameter	Symbol	Min	Max	Unit	Note/Test condition
Input high voltage	VIH	0,7 × VDD	VDD + 0,5	V	
Input low voltage	VIL	-0,5	0,3 × VDD	V	
Output high voltage	VOH	0,9 × VDD		V	IOH = -100 uA
Output low voltage	VOL		0,1 × VDD	V	IOL = 1,0 mA
SPI_NSS Low Level Output current (see note)	IOL	-1	-	mA	VOL = 0,3 V
Maximal SPI_NSS line capacitance (see note)	Cl	-	20	pF	
NOTE: Applicable for the physical interface with 4 signals.					

Table 6.3: DC characteristics for operational voltage class C

Parameter	Symbol	Min	Max	Unit	Note/Test condition
Input high voltage	VIH	0,7 × VDD	VDD + 0,3	V	
Input low voltage	VIL	-0,3	0,3 × VDD	V	
Output high voltage	VOH	0,9 × VDD		V	IOH = -100 uA
Output low voltage	VOL		0,1 × VDD	V	IOL = 1,0 mA
SPI_NSS Low Level Output current (see note)	IOL	-1	-	mA	VOL = 0,3 V
Maximal SPI_NSS line capacitance (see note)	Cl	-	20	pF	
NOTE: Applicable for the physical interface with 4 signals.					

The value of the resistor R in figure 6.2 shall be selected for a resultant maximum current lower than or equal to the minimum between the absolute IOL values of the master and the slave.

6.4.2 Data transfer mode, AC characteristics

The SPI interface shall implement the SPI mode 0 according to the industry de-facto SPI specification.

SPI mode 0 is determined by CPOL = 0 and CPHA = 0 where:

- CPOL: defines the SPI_CLK idle state.
- CPOL = 0 implies that the SPI_CLK is at input low voltage while it is idle.
- CPHA: defines the data sampling time.
- CPHA = 0 implies that data sampling is done on the rising edges of the SPI_CLK for both SPI_MISO and SPI_MOSI.

SPI_NSS is considered active or asserted at low voltage level.

Data availability timings with reference to SPI_CLK are shown in figure 6.3.