INTERNATIONAL STANDARD

First edition 2013-02-01

Road vehicles— FlexRay communications system —

Part 3: Data link layer conformance test specification

iTeh STVéhicules routiers — Système de communications FlexRay —

Partie 3: Spécification d'essai de conformité de la couche de liaison de données

ISO 17458-3:2013 https://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29fab328bf0fca0/iso-17458-3-2013



Reference number ISO 17458-3:2013(E)

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>ISO 17458-3:2013</u> https://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29fab328bf0fca0/iso-17458-3-2013



COPYRIGHT PROTECTED DOCUMENT

© ISO 2013

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office Case postale 56 • CH-1211 Geneva 20 Tel. + 41 22 749 01 11 Fax + 41 22 749 09 47 E-mail copyright@iso.org Web www.iso.org

Published in Switzerland

Contents

Introduction v 1 Scope 1 2 Normative references 1 3 Terms, definitions, symbols and abbreviated terms 1 3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 1 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 7.3 Internal RXDelay pehros F.A.N.D.A.R.D. PREV/F.W. 9 6.4 Analog delays 9 6.5 Accepted deviations (standardesitch:ai) 7 Conformance test cases structure	Forewo	ord	iv
1 Scope 1 2 Normative references 1 3 Terms, definitions, symbols and abbreviated terms 1 3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 2 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 7.3 Internal RXDelay Febr STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Test architecture 6 6.6 Testability requirements 10 6.6 Testability requirements 10 6.7 Receive data 25 7.0 forformance test cases subtroucture 25 7.4 Clock synchronisation 46 7.5 Makeup 50 7.6 Miscellaneous 62 <	Introdu	iction	v
2 Normative references 1 3 Terms, definitions, symbols and abbreviated terms 1 3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 2 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.1 Test architecture 6 6.2 Test implementation 7 7 Internal RXDelays 9 6.4 Analog delays 9 6.5 Accepted deviations (st an d and stitch.ai) 7 Conformance test cases 10 6.6 Testability requirements 11 7.1 Conformance test case structure 30 7.2 Receive data 23 7.3 Clock synchronisation 40 7.4 Clock synchronisation 40 7.5 Wakeup 30 7.6 Startup <td< td=""><td>1</td><td>Scope</td><td> 1</td></td<>	1	Scope	1
2 Normative references 1 3 Terms and definitions 1 3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test implementation 7 6.3 Internal RXDelay Context Co	ว		
3 Terms, definitions, symbols and abbreviated terms 1 3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 4 4 Conventions 4 5 Document overview. 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation. 7 6.3 Instrait RxDelay Febro STANDARD PREVEEW 9 6.4 Analog delays 9 6.5 Accepted deviations	Z	Normative references	1
3.1 Terms and definitions 1 3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 7.3 Internal RXDelayF ent STANDARD PREVIEW 9 9.4 Analog delays 9 6.5 Accepted deviations (standards.iten.ai) 10 6.6 Testability requirements 10 6.1 Test execution 11 11 6.7 Receive data 23 23 7.3 Charact statements and test case structure access and structure access access access access	3	Terms, definitions, symbols and abbreviated terms	1
3.2 Symbols 1 3.3 Abbreviated terms 2 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RXDelay Febrer STANDARD PREVIEW 9 6.4 Analog delays 6 6.5 Cested deviations (standards, steh, ai) 6.6 Testability requirements 10 6.6 Testability requirements 11 6.7 Test execution ISO 17458-32010 7 Conformance test cases structure 14 7 Conformance test cases structure 23 7.3 CHI 125 7.4 Clock synchronisation 440 7.5 Wakeup 530 7.6 Statup 530 7.7 Miscellaneous 672 7.8 Optional TT-E feature 620 7.9 Preambles <td< td=""><td>3.1</td><td>Terms and definitions</td><td> 1</td></td<>	3.1	Terms and definitions	1
3.3 Abbreviated terms 2 3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RXDelay Center STATUDARD PREVIEW 9 6.4 Analog delays 10 6.5 Accepted deviations (standards.itch.ai) 10 6.6 Test execution 11 11 6.7 Test execution 11 11 7 Conformance test cases structure use structure uses st	3.2	Symbols	1
3.4 Functions 4 4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RxDelay Febres TANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations (standards.itch.ai) 10 6.6 Testability requirements 11 10 6.7 Testability requirements 11 11 6.7 Conformance test cases structure to the structu	3.3	Appreviated terms	2
4 Conventions 4 5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RxDelay Febr STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations (standards.itch.ai) 6.6 Testability requirements 10 6.6 Test execution Iso 17458-32013 7 Conformance test cases Iso 17458-32013 7.1 General statements and test case structure iso event 16 7.2 Receive data 23 7.3 CHI 125 7.4 Clock synchronisation 440 7.5 Wakeup 530 7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.1	3.4	Functions	4
5 Document overview 5 6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RxDelay Febrer STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations (standards.itch.ai) 10 6.6 Testability requirements 11 11 6.7 Test execution 10 11 6.7 Test execution 10 11 7.7 Conformance test cases interments intermentation of the event of	4	Conventions	4
6 General 6 6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RxDelay Ed. STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations (standards.itch.ai) 10 6.6 Testability requirements 11 6.7 Test execution 14 7 Conformance test cases 10 7.1 General statements and test case structure uses account in the structu	5	Document overview	5
6.1 Test architecture 6 6.2 Test implementation 7 6.3 Internal RxDelay Feb STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations (standards.itch.ai) 10 6.6 Test execution 11 11 6.7 Test execution 14 150 (7458-32013) 14 7 Conformance test cases international and test case (structure upon 2000 child) (cloube) 16 7.1 General statements and test case structure upon 2000 child) (cloube) 16 7.2 Receive data 23 7.3 CHL 125 7.4 Clock synchronisation 440 7.5 Wakeup 568 7.6 Startup 568 7.7 Optional TT-E feature 820 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test	6	General	6
6.2 Test implementation	6.1	Test architecture	6
6.3 Internal RxDelay Eth STANDARD PREVIEW 9 6.4 Analog delays 9 6.5 Accepted deviations 10 6.6 Testability requirements 11 6.7 Test execution 14 7 Conformance test cases 16 7.1 General statements and test case structure to some the some test case structure to some test cases 16 7.2 Receive data 23 7.3 CHI 125 7.4 Clock synchronisation 440 7.5 Wakeup 530 7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Static test cases 861 9.3 Static test cases 861	6.2	Test implementation	7
6.4 Analog delays 9 6.5 Accepted deviations	6.3	Internal RxDelayColor STANDADD DDCX/ICXX	9
6.5 Accepted deviations	6.4	Analog delays	9
6.6 Testability requirements 11 6.7 Test execution 10 14 14 14 7 Conformance test cases structure users and test case structure	6.5	Accepted deviations	10
6.7 Test execution 14 7 Conformance test cases structure and second	6.6	Testability requirements	11
ISO 17458-32013 16 Conformance test cases intractionation with the wave 5000 doits of the total bases. 16 Receive data 23 7.3 CHI 125 7.4 Clock synchronisation 440 7.5 Wakeup 530 7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 9.2 Protocol parameter 861 9.3 Normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865	6.7	Test execution	14
7 Conformance test cases intractive sectors in the sector of the sec	-	<u>ISO 17458-3:2013</u>	40
7.1 General statements and test case, structure, 138-3-2013 10 7.2 Receive data	1	Conformance test cases ich ai cataby/standards/sist/259ac968-dbd9-4c10-b29f-	16
7.2 Receive data 23 7.3 CHI 125 7.4 Clock synchronisation 440 7.5 Wakeup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 9.2 Protocol parameter 861 9.1 Electrical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865 865	7.1	General statements and test case structure 458-3-2013	10
7.3 CHI	7.2		23
7.4 Clock synchronisation 440 7.5 Wakeup 530 7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 8.1 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865 865	7.3	CHI	125
7.5 Wakeup 530 7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography. 865 865	7.4	Clock synchronisation	440
7.6 Startup 568 7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865 865	7.5	Wakeup	530
7.7 Miscellaneous 672 7.8 Optional TT-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 8.1 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865 865	7.6	Startup	568
7.8 Optional 11-E feature 820 7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 9.3 Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 864 864	1.1		6/2
7.9 Preambles 846 8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication 60 864 Bibliography 865 865	7.8		820
8 Configuration 854 8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication 862 864 Bibliography 865	7.9	Preambles	846
8.1 Basic configuration 854 8.2 Standard modifications 859 9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 Bibliography 865 865	8	Configuration	854
8.2 Standard modifications	8.1	Basic configuration	854
9 Static test cases 861 9.1 Electrical interface 861 9.2 Protocol parameter 861 Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 862 Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0 864 8ibliography 865	8.2	Standard modifications	859
9.1 Electrical interface	9	Static test cases	861
9.2 Protocol parameter	9.1	Electrical interface	861
Annex A (normative) Technical data for the electrical interface of a FlexRay Communication Controller V3.0	9.2	Protocol parameter	861
Controller V3.0	Annex	A (normative) Technical data for the electrical interface of a FlexRay Communication	
Annex B (normative) Technical data for the protocol parameter of a FlexRay Communication Controller V3.0		Controller V3.0	862
Controller V3.0	Annoy	B (normative) Technical data for the protocol parameter of a Elex Pay Communication	
Bibliography	AIIIIeX	Controller V3.0	864
	Bibliog	Jraphy	865

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of technical committees is to prepare International Standards. Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights.

ISO 17458-3 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 17458 consists of the following parts, under the general title *Road vehicles* — *FlexRay communications* system: (standards.iteh.ai)

- Part 1: General information and use case definition ISO 17458-3:2013
- Part 2: Data link layer specification ab328bf0fca0/iso-17458-3-2013
- Part 3: Data link layer conformance test specification
- Part 4: Electrical physical layer specification
- Part 5: Electrical physical layer conformance test specification

Introduction

The FlexRay communications system is an automotive focused high speed network and was developed with several main objectives which were defined beyond the capabilities of established standardized bus systems like CAN and some other proprietary bus systems. Some of the basic characteristics of the FlexRay protocol are synchronous and asynchronous frame transfer, guaranteed frame latency and jitter during synchronous transfer, prioritization of frames during asynchronous transfer, single or multi-master clock synchronization, time synchronization across multiple networks, error detection and signalling, and scalable fault tolerance.

The FlexRay communications system is defined for advanced automotive control applications. It serves as a communication infrastructure for future generation high-speed control applications in vehicles by providing:

- A message exchange service that provides deterministic cycle based message transport;
- Synchronization service that provides a common time base to all nodes;
- Start-up service that provides an autonomous start-up procedure;
- Error management service that provides error handling and error signalling;
- Wakeup service that addresses the power management needs.V + + + +

Since start of development the automotive industry world wide supported the specification development. The FlexRay communications system has been successfully implemented in production vehicles today.

The ISO 17458 series specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called "FlexRay communications system".

This part of ISO 17458 has been established in order to define the protocol conformance test case requirements.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1 and ISO/IEC 10731, which structures communication systems into seven layers. When mapped on this model, the protocol and physical layer requirements specified by ISO 17458 are broken into:

- Diagnostic services (layer 7), specified in ISO 14229-1 [14], ISO 14229-4 [16];
- Presentation layer (layer 6), vehicle manufacturer specific;
- Session layer services (layer 5), specified in ISO°14229-2 [15];
- Transport layer services (layer 4), specified in ISO 10681-2 [5];
- Network layer services (layer 3), specified in ISO 10681-2 [5];
- Data link layer (layer 2), specified in ISO 17458-2, ISO 17458-3;
- Physical layer (layer 1), specified in ISO 17458-4, ISO 17458-5;

in accordance with Table 1.

Applicability OSI 7 layers		ISO 17458 FlexRay communications system	Vehicle manufacturer enhanced diagnostics	
	Application (layer 7)	vehicle manufacturer specific	ISO 14229-1, ISO 14229-4	
Sovenlaver	Presentation (layer 6)	vehicle manufacturer specific	vehicle manufacturer specific	
according to	Session (layer 5)	vehicle manufacturer specific	ISO 14229-2	
ISO 7498-1 and	Transport (layer 4)	vehicle manufacturer specific	150 10691 2	
ISO/IEC	Network (layer 3)	vehicle manufacturer specific	130 10001-2	
10731	Data link (layer 2)	ISO 17458-2, IS	SO 17458-3	
	Physical (layer 1)	ISO 17458-4, IS	SO 17458-5	

Table 1 — FlexRay communications system specifications applicable to the OSI layers

Table 1 shows ISO 17458 Parts 2 – 5 being the common standards for the OSI layers 1 and 2 for the FlexRay communications system and the vehicle manufacturer enhanced diagnostics.

The FlexRay communications system column shows vehicle manufacturer specific definitions for OSI layers 3-7.

The vehicle manufacturer enhanced diagnostics column shows application layer services covered by ISO 14229-4 which have been defined in compliance with diagnostic services established in ISO 14229-1, but are not limited to use only with them, ISO 14229-4 is also compatible with most diagnostic services defined in national standards or vehicle manufacturer's specifications. The presentation layer is defined vehicle manufacturer specific. The session layer services are covered by ISO 14229-2. The transport protocol and network layer services are specified in ISO 10681.

ISO 17458-3:2013 https://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29fab328bf0fca0/iso-17458-3-2013

Road vehicles — FlexRay communications system — Part 3: Data link layer conformance test specification

1 Scope

This part of ISO 17458 specifies the FlexRay protocol conformance test. This test verifies the conformance of FlexRay communication controllers with respect to ISO 17458-2.

Some testability requirements are given in 6.2.2.3 and 6.6 and are applicable for FlexRay communication controllers to pass the conformance test

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies. A RD PREVIEW

ISO 17458-2, Road vehicles — FlexRay communications system — Part 2: Data link layer specification

ISO 17458-4, Road vehicles — FlexRays communications system — Part 4: Electrical physical layer specification https://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29fab328bf0fca0/iso-17458-3-2013

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions defined in ISO 17458-2 and ISO 17458-4 apply.

3.2 Symbols

Δ	delta
E	Element, lower-case epsilon
ξ	Xsi
μΤ	microtick
σΤ	gdSampleClockPeriod (= Sampletick)
t _{RC}	modification of cycle length due to calculated rate correction (equal to <i>zRateCorrection</i> , used in figures of "Clock synchronisation")
<i>t</i> oc	modification of cycle length due to calculated offset correction (equal to <i>zOffsetCorrection</i> , used in figures of "Clock synchronisation")

ISO 17458-3:2013(E)

- $\boldsymbol{\varphi}_{\mathsf{Rx}}, \, \boldsymbol{\varphi}_{\mathsf{Tx}}$ analogue delays (see 6.4)
- ξ , ξ_{IUT} allowed deviation from theoretical results due to LT-IUT jitter (see 6.5)

3.3 Abbreviated terms			
BC	basic configuration		
BD	bus driver		
BSS	byte start sequence		
CAS	collision avoidance symbol		
СС	communication controller		
CE	communication element		
СНІ	controller host interface		
CHIRP	channel idle recognition point		
CRC	cyclic redundancy code		
DC	dual channel iTeh STANDARD PREVIEW		
DTS	dynamic trailing sequence (standards.iteh.ai)		
FES	frame end sequence ISO 17458-3:2013		
FIFO	first in first outtps://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29f- ab328bf0fca0/iso-17458-3-2013		
FPGA	field programmable gate array		
FSS	frame start sequence		
ID	identifier		
IP	intellectual property		
IUT	implementation under test		
LT	lower tester		
MT	macrotick		
MTS	media access test symbol		
NIT	network idle time		
NM	network management		
PE	protocol engine		
POC	protocol operation control		
RTL	register transfer level		

RxD	receive data signal from bus driver
SC	single channel
TE	test execution
TSS	transmission start sequence
TT-D	time triggered distributed
TT-E	time triggered external
TxD	transmit data signal from CC
TxEN	transmit data enable not signal from CC
UT	upper tester
WUDOP	wakeup during operation pattern
WUP	wakeup pattern
WUS	wakeup symbol
POC states:	iTeh STANDARD PREVIEW
С	POC:config (standards.iteh.ai)
CSCC	POC:coldstart consistency check
CSCR	POC:coldstart.collision/resolution.dards/sist/259ac968-dbd9-4c10-b29f-
CSG	ab328bi0ica0/iso-1/458-3-2013 POC:coldstart gap
CSJ	POC:coldstart join
CSL	POC:coldstart listen
DC	POC:default config
н	POC:halt
ICC	POC:integration consistency check
ICSC	POC:integration coldstart check
IL	POC:integration listen
IS	POC:initialize schedule
NA	POC:normal active
NP	POC:normal passive
R	POC:ready

3.4 Functions

TruncateTowardsZero: function returns the integer part of a number without its fractional digits (= sign(x) * floor(|x|))

4 Conventions

ISO 17458 are based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical and data link layer (protocol).

iTeh STANDARD PREVIEW (standards.iteh.ai)

ISO 17458-3:2013 https://standards.iteh.ai/catalog/standards/sist/259ac968-dbd9-4c10-b29fab328bf0fca0/iso-17458-3-2013

5 Document overview

Figure 1 depicts the FlexRay document reference according to OSI model.



Figure 1 — FlexRay document reference according to OSI model

6 General

6.1 Test architecture

This part of ISO 17458 is based on a test architecture as shown in Figure 2, which follows the ISO 9646 standard. The implementation under test (IUT) is the FlexRay CC. The upper tester (UT) is connected to the FlexRay controller host interface (CHI) of the IUT and the CHI is device specific. The lower tester (LT) is connected to the FlexRay physical layer interface of the IUT and ISO 17458-4 describes this interface. The test coordination procedure controls the UT and the LT.

In a hardware-based test environment (see 6.2.2), the FlexRay CC can be an "embedded" FlexRay CC meaning that CC is embedded in a microcontroller. In this case, the CHI (i.e., the upper tester interface) is between the embedded FlexRay CC and the microcontroller and in order to get access to the CHI, the upper tester may be partly distributed to the microcontroller.

The test architecture shown in Figure 2 is suitable for testing one FlexRay CC.



Figure 2 — Standard test architecture

There are some optional test cases in this part of ISO 17458 which tests the optional TT-E feature by using a pair of FlexRay CCs, namely a source CC and a sink CC, which are connected via the time gateway interface. Here, the IUT is the pair of connected FlexRay CCs. To test the TT-E feature, the test architecture as shown in Figure 3 is proposed. The upper tester and lower tester are connected to both FlexRay CCs and the test coordination procedure controls the upper and lower tester.



6.2 Test implementation

6.2.1 General

The test cases and the proposed test architecture of this specification can be either implemented in a hardware-based environment or in a simulation-based environment. In the following, both environments are described.

6.2.2 Hardware-based test implementation

6.2.2.1 IUT

In a hardware-based test implementation, the IUT is a physical device. The IUT can be either a standalone FlexRay CC, an embedded FlexRay CC, or a FlexRay CC programmed in an FPGA. For testing the optional TT-E feature, the IUT consists of a pair of connected FlexRay CCs.

6.2.2.2 Lower tester

The electrical characteristics of the lower tester shall follow the electrical characteristics of the interface between the FlexRay CC and the FlexRay Bus Driver on the Bus Driver side. This interface is described in ISO 17458-4. The requirements on the lower tester in a hardware-based test environment, including the electrical characteristics, are listed in Table 2. It is not advised to use any extra circuits (e.g., level shifters) between the IUT's FlexRay CC and the lower tester.

Description	Relevant signal	Parameter name used in ISO 17458-4	Min	Max	Unit
Input capacitance	TxD, TxEN	C_BDTxD	-	10	pF
Threshold for detecting logical high	TxD, TxEN	uBDLogic_1	-	60	%
Threshold for detecting logical low	TxD, TxEN	uBDLogic_0	40	-	%
Voltage reference for logical high and low	TxD, TxEN, RxD	uVDIG	same as IUT		V
Sample Rate	TxD, TxEN	N/A	160	-	MHz
Asymmetry	RxD	see ISO 17458-4: measured at 50 % <i>uVDIG</i> and 25 pF load	-	2	ns
Sum of rise and fall time @ 15 pF load	RxD	dBDRxDR15 + dBDRxDF15	-	13	ns
Difference of rise and fall time @ 15 pF load	RxD	dBDRxDR15 – dBDRxDF15	-	5	ns
Sum of rise and fall time @ 25 pF load	RxD	dBDRxDR25 + dBDRxDF25	-	16,5	ns
Difference of rise and fall time @ 25 pF load	RxD	dBDRxDR25 – dBDRxDF25	-	5	ns
Frequency of FlexRay clock, provided to IUT	clk	N/A	-	80	MHz
Precision of FlexRay clock, provided to UT		NAD PREVIEW	-	500	ppm

Table 2 — Requirements on the lower tester in a hardware-based test environment

(stanuarus.iten.ai)

6.2.2.3 **Clock synchronisation**

ISO 17458-3:2013

Several test cases require the synchronisation between the IUTs and the test environment such that random clock deviations can be excluded and the occurrence time of a sampletick can be determined within one sampletick accuracy.

Therefore it is required that the LT provides a clock signal (called "FlexRay clock") to the IUT. The LT shall use the FlexRay clock as a basis for FlexRay bus stimuli of the RxD signal and for sampling the TxD and TxEN signals. The IUT shall also use the FlexRay clock for FlexRay transmission and reception. Existing PLLs in the IUT need to be bypassed or programmed not to multiply. If the IUT uses an own clock source or an active PLL, then there might be the risk of failing some test cases.

Some requirements on the FlexRay clock signal are listed in Table 2. In addition, those frequencies shall be supported, which can be derived from 80 MHz by integer division. The FlexRay clock shall run continuously in order to be able to test embedded FlexRay CCs, where the FlexRay clock signal is also used to for clocking the host microcontroller.

6.2.3 Simulation-based test implementation

In a simulation-based test implementation, the IUT is described in a hardware description language typically on register transfer level (RTL), e.g., in SystemVerilog code or VHDL code. The IUT is a FlexRay CC, including message buffers and FIFO. For testing the optional TT-E feature, the IUT consists of a pair of connected FlexRay CCs. The test environment (upper tester, lower tester, and test coordination procedure) and the test cases exist as software only. Executing a test case in a simulation-based test implementation means to load all necessary parts (IUT, test environment, test case) in an RTL simulator and then to run the simulation.

In the simulation-based test implementation, the clocks of the IUT and the LT have no deviation from the nominal frequency and also have no jitter. Therefore, no requirements on the clock synchronisation between the LT and the IUT (as listed in 6.2.2.3 for the hardware-based test implementation) are given for the simulation-based test implementation. However, ξ_{IUT} and ξ (see 6.5) have to be considered in the simulation-based test implementation.

6.3 Internal RxDelay

The parameter *adInternalRxDelay* is implementation specific and has an allowed range between 1 and 4 sampleticks ISO 17458-4. All basic configurations (see clause 8) assume *adInternalRxDelay* to be 4 sampleticks. In order to compensate between the implementation specific value of *adInternalRxDelay* and the assumed value of 4 sampleticks, a delay compensation shall be integrated in the RxD signal between the LT and the IUT. The delay compensation shall have a delay of 4-dt [sampleticks], and dt is the IUT's actual value of *adInternalRxDelay*. The delay compensation shall be applied in the hardware-based test implementation. Figure 4 gives an example how to implement the delay compensation in a hardware-based test implementation.

Please note that in the test cases, the time interval between IUT's frame and LT's frame are measured at the test points marked in Figure 4. Therefore the delay compensation is not to be considered in test steps like *"It is verified (LT) that the interval between the IUT's frames in slot 1 and LT's frame slot 2 is x \muT...".*

Figure 4 depicts the proposal for compensation of *adInternalRxDelay* in a hardware-based test implementation.



Figure 4 — Proposal for compensation of adInternalRxDelay in a hardware-based test implementation

6.4 Analog delays

Analog delays of the IUT appear in the signal paths between the physical pads of the device and the flip flops of the FlexRay CC. In ISO 17458-4, the analog delays are captured in the following parameters: dCCRxD01, dCCTxD01, dCCTxD01, dCCTxD10, dCCTxEN10 or dCCTxEN01. In this conformance test specification, the following two analog delays are defined: φ_{Rx} is the analog delay on the reception path, and φ_{Tx} is the analog delay on the transmission path. In the hardware-based test implementation, the analog delays are determined as follows:

- $-- \varphi_{\mathsf{Rx}} \in [0; \max\{dCCRxD01, dCCRxD10\}]$
- $-- \varphi_{\mathsf{Tx}} \in [0; \max\{dCCTxD01, dCCTxD10, dCCTxEN10, dCCTxEN01\}]$