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Road vehicles— FlexRay communications system —

Part 4: Electrical physical layer specification

Véhicules routiers — Système de communications FlexRay —

Partie 4: Spécification de la couche d'application électrique

Reference number
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Foreword

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The main task of technical committees is to prepare International Standards. Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights.

ISO 17458-4 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 17458 consists of the following parts, under the general title *Road vehicles — FlexRay communications system*:

— *Part 1: General information and use case definition*

— *Part 2: Data link layer specification*

— *Part 3: Data link layer conformance test specification*

— *Part 4: Electrical physical layer specification*

— *Part 5: Electrical physical layer conformance test specification*

Introduction

The FlexRay communications system is an automotive focused high speed network and was developed with several main objectives which were defined beyond the capabilities of established standardized bus systems like CAN and some other proprietary bus systems. Some of the basic characteristics of the FlexRay protocol are synchronous and asynchronous frame transfer, guaranteed frame latency and jitter during synchronous transfer, prioritization of frames during asynchronous transfer, single or multi-master clock synchronization, time synchronization across multiple networks, error detection and signalling, and scalable fault tolerance.

The FlexRay communications system is defined for advanced automotive control applications. It serves as a communication infrastructure for future generation high-speed control applications in vehicles by providing:

- A message exchange service that provides deterministic cycle based message transport;
- Synchronization service that provides a common time base to all nodes;
- Start-up service that provides an autonomous start-up procedure;
- Error management service that provides error handling and error signalling;
- Wakeup service that addresses the power management needs.

Since start of development the automotive industry world-wide supported the specification development. The FlexRay communications system has been successfully implemented in production vehicles today.

The ISO 17458 series specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called "FlexRay communications system".

This part of ISO 17458 has been established in order to define the electrical physical layer of the FlexRay data link.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1 and ISO/IEC 10731, which structures communication systems into seven layers. When mapped on this model, the protocol and physical layer requirements specified by ISO 17458 are broken into:

- Diagnostic services (layer 7), specified in ISO 14229-1 [7], ISO 14229-4 [9];
- Presentation layer (layer 6), vehicle manufacturer specific;
- Session layer services (layer 5), specified in ISO 14229-2 [8];
- Transport layer services (layer 4), specified in ISO 10681-2 [1];
- Network layer services (layer 3), specified in ISO 10681-2 [1];
- Data link layer (layer 2), specified in ISO 17458-2, ISO 17458-3;
- Physical layer (layer 1), specified in ISO 17458-4, ISO 17458-5;

in accordance with Table 1.

Table 1 — FlexRay communications system specifications applicable to the OSI layers

Applicability	**OSI 7 layers**	**FlexRay communications system**	**Vehicle manufacturer enhanced diagnostics**
Seven layer according to ISO 7498-1 and ISO/IEC 10731	Application (layer 7)	vehicle manufacturer specific	ISO 14229-1, ISO 14229-4
	Presentation (layer 6)	vehicle manufacturer specific	vehicle manufacturer specific
	Session (layer 5)	vehicle manufacturer specific	ISO 14229-2
	Transport (layer 4)	vehicle manufacturer specific	ISO 10681-2
	Network (layer 3)	vehicle manufacturer specific	
	Data link (layer 2)	ISO 17458-2, ISO 17458-3	
	Physical (layer 1)	ISO 17458-4, ISO 17458-5	

Table 1 shows ISO 17458 Parts 2 – 5 being the common standards for the OSI layers 1 and 2 for the FlexRay communications system and the vehicle manufacturer enhanced diagnostics.

The FlexRay communications system column shows vehicle manufacturer specific definitions for OSI layers 3 – 7.

The vehicle manufacturer enhanced diagnostics column shows application layer services covered by ISO 14229-4 which have been defined in compliance with diagnostic services established in ISO 14229-1, but are not limited to use only with them. ISO 14229-4 is also compatible with most diagnostic services defined in national standards or vehicle manufacturer's specifications. The presentation layer is defined vehicle manufacturer specific. The session layer services are covered by ISO 14229-2. The transport protocol and network layer services are specified in ISO 10681.

Road vehicles — FlexRay communications system — Part 4: Electrical physical layer specification

1 Scope

This part of ISO 17458 specifies the electrical physical layer for FlexRay communications systems.

The electrical physical layer for FlexRay is designed for time-triggered networks with data-rates up to 10 Mbit/s to connect automotive electronic control units (ECUs). The medium that is used is dual wires. Signalling on the bus is accomplished by asserting a differential voltage between those wires. Topology variations range from point-to-point connections via linear passive busses and passive stars up to active star topologies.

This part of ISO 17458 includes the definition of electrical characteristics of the transmission itself and also documentation of basic functionality for bus driver (BD) and active star (AS) devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17458-1, *Road vehicles — FlexRay communications system — Part 1: General information and use case definition*

ISO 17458-2, *Road vehicles — FlexRay communications system — Part 2: Data link layer specification*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 17458-1, ISO 17458-2 and the following apply.

3.1.1
alternating current busload
AC busload
equivalent circuit of a passive star from transmitting view of the bus driver

3.1.2
active elements
components which work with power supply and amplifiers

3.1.3
active star network
AS network
all *point-to-point* connections plugged to an *AS*

3.1.4
activity
See "*bus state*"
NOTE activity distinguishes two states: *Data_0* and *Data_1.*

3.1.5
Activity
signal to the Central_Logic when this *communication path* is not *idle(*see also *NoActivity)*

3.1.6
asymmetric delay budget
maximum bit-deformation in the time domain

NOTE It is derived from the specified synchronization and sampling procedure and the properties of their implementation. When transmitting a FlexRay data stream the receiving CC must be able to detect the data without any error. If the *asymmetric delay* of the data stream is higher than the *asymmetric delay budget*, the decoder samples faulty bit values.

3.1.7
asymmetric delay
bit-deformation in the time domain when passing a data stream e.g. via a *BD*

EXAMPLE

A data steam is applied to the BD´s input TxD: …00100

The single 1 at the centre shall have a length of 100 ns.
The *BD* passes the data stream to its output *BP* and *BM*.
The single 1 may be shortened or lengthened a little bit to e.g. 102 ns.
In this case the *asymmetric delay* has to be determined to 2 ns.

3.1.8
bus driver – bus driver interface
BD-BD-interface
consideration of all involved effects of the timing of each *BD*/*AS*

NOTE The timing is specified based on measurement set-ups easy to be used. When connecting two *BDs*/*AS*s (via e.g. a *passive star*) the resulting delays are not equal to twice the specified values.

3.1.9
bus guardian enable
BGE
input pin of the *BD that* allows deactivating the bus output stage of the *BD*

3.1.10
bias voltage
voltage source with high output impedance

3.1.11
bus minus
BM
bidirectional pin of the *BD*/*AS* to allow the *BD*/*AS* the access to the bus.

3.1.12
bus plus
BP
bidirectional pin of the *BD*/*AS* to allow the *BD*/*AS* the access to the bus.

3.1.13
branch
component within *active star topologie*s

NOTE A *branch* can be built of a *point-to-point* connection, a *linear bus* or a *passive star*.

3.1.14
byte start sequence
BSS
pre-defined sequence of two bits (logical: 10) which is sent in front of each byte

3.1.15
bus guardian
BG
component which allows the node only to transmit during the pre-defined timing slots

3.1.16
bus state
status of the bus FlexRay communication

NOTE Several different states are visible due to the operating modes of the FlexRay system.

EXAMPLE

idle: there is no communication on the bus. Approximately 0 V differential voltage is measurable.
activity: there is an on-going communication on the bus. Approximately ±600 mV up to ±1 000 mV differential voltage is measurable, etc.

3.1.17
cascade
topology character

NOTE If a topology uses more than 1 *AS* the wording "*cascaded ASs*" is used.

3.1.18
common mode
mode in which two test points are handled simultaneously against ground

EXAMPLE

common mode input impedance of the *BD*´s bus pins *BP* and *BM* to ground.
common mode voltage on the bus: ½ (*uBP* + *uBM*)

3.1.19
communication path
branches CC interface and Intra Star Interface

3.1.20
connection network
components like CMC, termination resistors, *ESD* protection circuits, lines on the *PCB*, connectors, etc

NOTE When implementing a FlexRay system each *BD*/*AS* has to be plugged to a FlexRay *cable* via these components.

3.1.21
Data_0
bus-state "*activity*""where a logical 0 is transmitted

3.1.22
Data_1
bus-state "*activity*"" where a logical 1 is transmitted.

3.1.23
differential mode
mode in which two test points are handled against each other

EXAMPLE

differential mode input impedance of the BD´s bus pins BP and BM to ground.
differential mode voltage on the bus: (*uBP* - *uBM*).
differential mode impedance of the FlexRay *cable*

3.1.24
dummy load
summary of loads that can be applied to components which are specified by easy-to-use measurement set-ups

EXAMPLE

dummy load at *BP* and *BM*: 40 Ω || 100 pF.
dummy load at *RxD*: 15 pF

3.1.25
eye-diagram
diagram that is visible when overlying edge synchronized measured bus signals

NOTE The shape of the eye allows specifying the bus-signals.

3.1.26
frame end sequence
FES
bit sequence that consists of two bits (01) and is sent at the end of each FlexRay data frame

NOTE The asymmetric delay budget is based on the end of a data frame: in the worst case up to 10 consecutive identical bits can be seen.
BSS + 1 byte + *FES* = 10 00000000 01

3.1.27
functional class
grouping of various features that are implemented together

NOTE The *BD*/*AS* offers various technical features. To keep the resulting products testable and to offer them a good chance on the market it is required to implement various features only together.

3.1.28
generic bus driver
simulation model which is derived from the specification directly

NOTE The knowledge about real implementations is taken into consideration. The generic *BD* supports a receiver stage, a transmitter stage and optionally the *AS* routing behaviour.

3.1.29
idle
see "*bus state*".
Idle distinguishes 3 bus biasing states:
idle while all nodes are neither un-powered nor in a low power mode, thus all nodes are biasing the bus.
idle while all nodes are either un-powered or in a low power, thus none of the nodes is biasing the bus.
idle while some nodes are biasing the bus and others not.

3.1.30
leg
passive network that is involved in the calculation of *timing budget*

NOTE A topology is interpreted as a single path from a transmitter to a receiver that contains several passive networks. Each of these passive networks is named *leg*.

3.1.31
linear passive bus
FlexRay bus that consists of 2 terminated FlexRay nodes with one *cable* between

NOTE Additionally some un-terminated FlexRay nodes are plugged to the cable by *splices* and short *stubs*.

3.1.32
monolithic
see: *active star*.

NOTE This term is used to characterize various implementations on an *AS*. If the *AS* is *monolithic* implemented all specified components are included in a single device.

3.1.33
NoActivity
signal to the Central_Logic when this communication path is *idle* is detected *(*see also *Activity)*

3.1.34
non-monolithic
character of various implementations on an *AS*

NOTE This term is used to characterize various implementations on an *AS*. If the *AS* is *non-monolithic* implemented all specified components are not included in a single device, two devices are used at least. See "*active star*".

3.1.35
NotReceiveActive
communication path signals *NotReceiveActive* to the Central_Logic when a state is entered at that the *communication path* is idle or is actively transmitting data

3.1.36
parasitic capacity
capacity that appears although it is not technically necessary

EXAMPLE

pins of a device housing generate a capacity

3.1.37
parasitic resistance
resistance that appears although it is not technically necessary

3.1.38
passive net
all possible implementation of *AS branches*

NOTE This summarizes: point-to-point connections, linear busses and passive stars. They do not include *BD*/*AS*s.

3.1.39
passive star network
network consisting of passive stars

3.1.40
physical layer
component that includes all components between *TP0* and *TP5*

3.1.41
ReceiveActive
communication path signals *ReceiveActive* to the Central_Logic when a state is entered at that the incoming data stream is forwarded to other *communication paths*

3.1.42
receiver
device or entity that receives an information transfer originated by a transmitter

NOTE A term that is used in various ways based on the context.

EXAMPLE

BD´s input stage from the bus.
FlexRay *communication element* receiving node

3.1.43
receive enable not
RxEN
output pin at the *BD* to show the state of the bus

NOTE Two states are distinguished: *idle* or *activity*

3.1.44
serial peripheral interface
SPI
synchronously working hardware interface to exchange data among circuits mounted on a *PCB*

3.1.45
signal integrity
SI
procedures or requirements to *differential* bus signals to guarantee the faultless transmission of FlexRay *communication elements*

3.1.46
signal integrity voting
SI voting
procedure to determine *Sq* based on measured *bus* signals

3.1.47
specific line delay
propagation of a FlexRay signal per meter of a transmission line in ns/m

3.1.48
splice
any implementation of a connection-point where 3 or more transmission lines are plugged together

NOTE A *splice* may contain passive components to damp radiation

EXAMPLE

A *splice* in a linear bus allows to connect a stub to a FlexRay node.

3.1.49
signal quality
Sq
parameter to describe whether the required *signal integrity* of FlexRay signals on the bus is met

NOTE Pass or fail are the possible results.

3.1.50
stochastic jitter
jitter of data stream edges in the time domain due to e.g. radiation

NOTE The EPL-specification passes its appropriate consideration to the responsible system designer.

3.1.51
stub
component within *passive net*s

NOTE A *stub* consists of a single FlexRay *cable* connected to the centre of a passive star or to a linear bus (short: plugged to a *splice*).
The *stub* ends at the BD pins BP and BM within a FlexRay node.

3.1.52
termination
set-up of components between a BD and a *transmission line*

NOTE Mainly they are used to ensure *SI* and *EMC* requirements.

EXAMPLE

Resistors, capacitances, chokes etc.

3.1.53
termination area (of the cables)
assembly of FlexRay *cables* to *ECU*-connectors that require several procedures which disturb the geometric integrity of the FlexRay *cable*:
untwisted, unshielded and unsheathed *cable* segment.
twisted but unshielded or unsheathed *cable* segment.
Both segments together represent the termination area.

3.1.54
test plane
virtual or real places to get electrical signals and to determine their properties

NOTE The *test planes* are located on the path from a transmitter to a receiver.

3.1.55
topology
non-hierarchical flat geometric structure of the FlexRay system

NOTE A distributed FlexRay system consists of several components like nodes, busses, active and passive stars etc.

3.1.56
test plane 0
TP0
virtual time reference point that represents the digital output from the protocol machine with a perfect timing according the data link layer specification

3.1.57
test plane 1 flip flop (virtual)
TP1_FFi
transmitting CC’s virtual test plane to visualize PLL jitter, clock skew and propagation delay of the flip flop

3.1.58
test plane 1 flip flop
TP1_FF
transmitting CC’s internal test plane at ‘Q’ pin of last flip flop before output buffer