SLOVENSKI STANDARD
SIST EN 150012:2002

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Blank detail specification: Single gate field-effect transistors

Blank Detail Specification: Single gate field-effect transistors

Vordruck für Bauartspezifikation: Feldeffekt-Transistoren mit einer Gate-Elektrode

Spécification particulière cadre: Transistors à effet du champ à grille unique

Ta slovenski standard je istoveten z: **EN 150012:1991**

ICS:

31.080.30 Tranzistorji Transistors

SIST EN 150012:2002 **en**

EUROPEAN STANDARD

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EN 150012

December 1991

UDC:

Descriptors: Quality, electronic components, transistors

English version

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This European Standard was approved by the CENELEC Electronic Components Committee (CECC) on 25 November 1991. The text of this standard consists of the text of CECC 50012 Issue 2 1980 of the corresponding CECC Specification. CENELEC members are bound to comply with CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the General Secretariat of the CECC or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CECC General Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and United Kingdom. The membership of the CECC is identical, with the exception of the national electrotechnical committees of Greece, Iceland and Luxembourg.

CECC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

blank

European Committee for Electrotechnical Standardization (CENELEC)
Cenelec Electronic Components Committee

CECC

English version

Harmonized System of Quality Assessment for
-Electronic Components

BLANK DETAIL SPECIFICATION:

SINGLE GATE FIELD-EFFECT TRANSISTORS

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:

TRANSISTORS A EFFET DE CHAMP A GRILLE UNIQUE

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK FÜR
BAUARTSPEZIFIKATION:

FELDEFFEKT-TRANSISTOREN MIT EINER GATE-ELEKTRODE

CECC 50012

1977

Contents

Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This document has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue detail specifications for FIELD-EFFECT TRANSISTORS. It should be read in conjunction with document CECC 00100: Basic Rules (1974).

At the date of printing of this document the member countries of the CECC are Belgium, Denmark, France, Germany, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom. Copies of this document can be obtained from the National Committees of the CENELEC in these countries.

Preface

This blank detail specification was prepared by CECC Working Group 5: "Semiconductor diodes and transistors".

It is one of a series of blank detail specifications for discrete semiconductor devices, all relating to the generic specification printed as CECC 50000.

The text of this specification was circulated to the CECC for voting in documents CECC (Secretariat) 463 and 584 in December 1975 and February 1977 respectively, and was ratified by the CECC for printing as a CECC Specification.

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

Contents

This blank detail specification is divided according to uses in a number of sections, as indicated hereafter. Each section is complete in itself in that all common parts have been repeated (e.g. limiting values).

blank

Section 1. Low frequency amplification

Numbers between square brackets on the next page correspond to the following indications which should be given:

Identification of the detail specification

[1] The name of National Standards Organization under whose authority the detail specification is drafted

[2] The CECC Symbol and the number allotted by the CECC General Secretariat to the completed detail specification

[3] The number and issue number of the national generic and sectional specifications

[4] The national number of the detail specification, date of issue and any further information required by the national system.

Identification of the component

[5] A short description of the type of component

[6] Information on typical construction (where applicable)

[7] Outline drawing and/or reference to the relevant document for outlines

[8] Application or group of applications covered (see note below)

[9] Reference data on the most important properties, to allow comparison between the various component types.

NOTE When a device is so designed that it can satisfy several applications, this should be stated in the detail specification, in which case the characteristic and inspection requirements relevant to these applications should be met simultaneously (these may appear in different columns of a blank detail specification or in different blank detail specifications, as the case may be).

[1]	page: of:	CECC 50012 Section 1 LF AMPLIFICATION	[2]
ELECTRONIC COMPONENT OF ASSESSED QUALITY IN ACCORDANCE WITH: [3]			[4]

DETAIL SPECIFICATION FOR: SINGLE GATE FIELD-EFFECT TRANSISTOR (S) [5]
TYPE-NUMBER (S):

CONSTRUCTION: Polarity: N-channel/P-channel

Device categories : Type A: junction-gate-type
Type B: insulated-gate depletion type
Type C: insulated-gate enhancement type

Case material : glass/metal/plastic/other [6]

1 Mechanical description [7]

Outline references (code A) from IEC 191-2:
National:

OR

Base and case references (codes B + C) from IEC 191-2:
National:

AND/OR

Outline drawing

TERMINAL CONNECTIONS: including any connections between terminals, case and substrate, if necessary

MARKING: letters and figures or colour code

2 Electrical application [8]

power : AMBIENT-RATED
frequency : LOW
use : AMPLIFICATION

3 Levels of quality assessment

F – L

4 Limiting values (absolute maximum system) COMMON TO ALL APPLICATIONS [9]

These apply over the operating temperature range, unless otherwise stated

				Types		
				A	B	C
4.1	Minimum and maximum ambient operating temperatures	T_{amb}	max min	x	x	x
4.2	Minimum and maximum storage temperatures	T_{stg}	max min	x	x	x
4.3	Maximum drain-source voltage under specified conditions	V_{DSX} (or V_{DSS} (or V_{DSR}	max	x	x	x
4.4	Maximum gate-source voltage (with $V_{DS} = 0$), reverse and, where appropriate, forward	V_{GSR} V_{GSF}	max max	x —	x (x)	x (x)
4.5	Maximum gate-drain voltage with source open-circuited	V_{GDO}	max	x	x	x
4.6	Maximum forward gate current	I_{GF}	max	x	—	—
4.7	Maximum drain current	I_D	max	x	x	x

See the relevant Qualified Products List for the availability of components qualified under this detail specification.

				Types		
				A	B	C
4.8	Power dissipation: Special requirements for ventilation/mounting should be specified					
4.8.1	Maximum total power dissipation as a function of temperature or:	$P_{tot\ max}$	vs T	x	x	x
4.8.2	Maximum virtual (equivalent) junction temperature and absolute limit of power dissipation	$T_{(Vj)}$ P_{tot}	max	x x	x x	x x
4.9	For insulated-gate devices with separate source and substrate terminals: (In general devices that include gate-protection diodes do not require this to be specified)					
4.9.1	Maximum gate-substrate voltage under specified conditions	$V_{GB}(V_{GU})$	max	—	x	x
4.9.2	Maximum drain-substrate voltage under specified conditions	$V_{DB}(V_{DU})$	max	—	x	x
4.9.3	Maximum source-substrate voltage under specified conditions	$V_{SB}(V_{SU})$	max	—	x	x

5 Characteristics (See 6 for inspection)

The characteristics marked x shall be given at T_{amb} = 25 °C unless otherwise stated.

Sign + indicates characteristic is verified under the inspection requirements.

Signs between brackets correspond to characteristics indicated "where appropriate", or given as alternatives.

			Types		
			A	B	C
5.1	Leakage or cut-off currents:				
	Either: maximum leakage or cut-off current with source open-circuited, preferably at maximum rated gate-drain voltage V_{GDO}	$I_{GDO\ (1)}$	(x)	(x)	(x)
	or: maximum leakage or cut-off current with drain short-circuited to source, preferably at maximum rated gate-source voltage V_{GSR}	$I_{GSS\ (1)}$	(x)	(x)	(x)
	or: maximum gate-source leakage or cut-off current, at specified V_{DS} and specified V_{GS} or I_D	I_{GS}	(x)	(x)	(x)
5.2	Leakage or cut-off currents at high temperature:				
	Either: maximum leakage or cut-off current with source open-circuited, at V_{GD} preferably between 65 % and 85 % of maximum rated V_{GDO} and at a high temperature (see **4.3.3** of CECC 50000)	$I_{GDO\ (2)}$	(x)	(x)	(x)
	or: maximum leakage or cut-off current with drain short-circuited to source, at V_{GS} preferably between 65 % and 85 % of maximum rated V_{GSR} and at a high temperature (see **4.3.3** of CECC 50000)	$I_{GSS\ (2)}$	(x)	(x)	(x)
5.3	Minimum and maximum gate-source cut-off voltage at specified V_{DS} and I_D (preferably ⩽ 1 μ A)	V_{GSoff}	x	x	—

				Types		
				A	B	C
+	5.4	Minimum and maximum drain current at $V_{GS} = 0$ and specified V_{DS} (d.c. or pulse as specified)	I_{DSS}	x	x	—
+	5.5	Minimum and maximum gate-source threshold voltage at specified V_{DS} and I_D	$V_{GS\,(TO)}$	—	—	x
+	5.6	Minimum and maximum drain current at specified V_{GS} and V_{DS}	I_D	—	—	x
+	5.7	Maximum short-circuit input capacitance at 1MHz, specified V_{DS} and specified V_{GS}	C_{11ss}	x	x	x
(+)	5.8	Where appropriate: Maximum short-circuit output conductance at specified frequency, specified V_{DS} and specified V_{GS} or I_D	g_{22ss}	(x)	(x)	(x)
+	5.9	Minimum and maximum short-circuit forward transconductance at specified frequency, specified V_{DS} and specified V_{GS} or I_D	y_{21s}	x	x	x
+	5.10	For low noise types only:				
		Maximum noise voltage or noise factor in common-source configuration, under specified conditions of bias, source resistance, centre frequency and power bandwidth.	V_n or F	x	x	x
	5.11	When virtual junction temperature is quoted as a rating: maximum value of thermal resistance junction to ambient	R_{th}(j-amb)	x	x	x

6 Test conditions and inspection requirements

These are given in the following tables, where the values and exact conditions to be used should be specified as required in the detail specification relevant to a given type in line with the indications given in CECC 50000 for the relevant test.

The tables refer to two levels of quality assessment arbitrarily designated F and L, it being understood that there may be other levels in other blank detail specifications.

All references to part numbers are made with respect to CECC 50000 unless otherwise stated.

GROUP A — Lot-by-lot

All tests are non destructive (**3.5.6** of CECC 50000)

AQL = given in %
⊕ 1 % if more than 3 tests

Examination or test		Ref.	Conditions at T_{amb} = 25 °C unless otherwise stated	Inspection requirements					
				Limits		Levels			
				Types A and B	Type C	F		L	
						IL	AQL	IL	AQL
SUB-GROUP A1						I	1,5	I	1,5
Visual inspection		**4.2.1**	**4.2.1**	**4.2.1**	**4.2.1**				
SUB-GROUP A2						II	0,65	II	0,65
Leakage or cut-off current (see **5.1** of this document)		**4.3.4** T-071		max	max		⊕		⊕
Either:									
	$I_{GDO\ (1)}$		V_{GD} = preferably V_{GDO} max I_S = 0						
or:	$I_{GSS\ (1)}$		V_{GS} = preferably V_{GSR} max V_{DS} = 0						
or:	I_{GS}		V_{DS} = specified V_{GS} or I_D = specified						
Gate-source cut-off voltage	V_{GSoff}	**4.3.4** T-074	V_{DS} = specified I_D = specified (preferably ⩽ 1 µA)	max min	—				
Drain current	I_{DSS}	**4.3.4** T-072	V_{DS} = specified V_{GS} = 0 d.c. or pulse as specified (note 1)	max min	—				
Gate-source threshold voltage	$V_{GS\ (TO)}$	**4.3.4** T-075	V_{DS} = specified I_D = specified	—	max min				
Drain current	I_D	**4.3.4** T-072	V_{DS} = specified V_{GS} = specified	—	max min				

NOTE 1 If pulse measurement is used, the conditions should preferably be: pulse width tp = 300 µs duty factor < 2 %

GROUP A — Lot-by-lot cont'd

All tests are non destructive (3.5.6 of CECC 50000) AQL = given in %

Examination or test	Ref.	Conditions at T_{amb} = 25 °C unless otherwise stated	Inspection requirements					
			Limits		Levels			
			Types A and B	Type C	F		L	
					IL	AQL	IL	AQL
SUB-GROUP A3					I	2,5	I	2,5
Short-circuit forward transconductance y_{21s}	4.3.4 T-078	V_{DS} = specified V_{GS} or I_D = specified f = specified	max min	max min				
SUB-GROUP A4					S4	4	S4	4
For low-noise types only:	4.3.4 T-079							
Noise factor F or		V_{DS} = specified V_{GS} or I_D = specified for low noise application	max	max				
Noise voltage V_n		R_G = specified bandwidth = specified f = specified						

GROUP B — Lot-by-lot

Only tests marked: (D) are destructive (**3.5.6** of CECC 50000)

LSL = lower specification limit (Group A) AQL = given in %

USL = upper specification limit (Group A) na = not applied

Examination or test	Ref.	Conditions at T_{amb} = 25 °C unless otherwise stated	Inspection requirements					
			Limits		Levels			
			Types A and B	Type C	F		L	
					IL	AQL	IL	AQL
SUB-GROUP B1 Dimensions	**4.2.2**	**4.2.2**/Appendix III	**4.2.2**	**4.2.2**	S2	2,5	S2	2,5
SUB-GROUP B3 Lead bending if applicable (D)	**4.4.9**	**4.4.9**	**4.4.9**	**4.4.9**	S3	2,5	S2	2,5
SUB-GROUP B4 Solderability	**4.4.7**	As specified	**4.4.7**	**4.4.7**	S4	2,5	S4	2,5
SUB-GROUP B5 Change of temperature followed by: accelerated damp heat (D) or sealing	**4.4.4** **4.4.2** **4.4.10**	As specified	V_{GSoff} and leakage current (A2) within original limits	$V_{GS\ (TO)}$	S4	2,5	na	na
SUB-GROUP B8 Electrical endurance (168 h)	**4.5**	**4.5.2.10** Electrical operation or high temperature reverse bias, as specified	V_{GSoff} $\geqslant$ 0,8 LSL and $\leqslant$ 1,2 USL leakage current (A2): $\leqslant$ 10 USL I_{DSS} $\geqslant$ 0,9 LSL and $\leqslant$ 1,1 USL	$V_{GS\ (TO)}$ I_D	S4	1,5	na	na
SUB-GROUP CTR	Attributes information for B3, B4, B5 and B8							