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Road vehicles — Local Interconnect Network (LIN) —

Part 7:
Electrical Physical Layer (EPL) conformance test specification

Véhicules routiers — Réseau Internet local (LIN) —

Partie 7: Spécification d'essai de conformité de la couche électrique physique (EPL)

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Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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The committee responsible for this document is ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Electrical and electronic equipment*.

A list of all parts in the ISO 17987 series can be found on the ISO website.

Introduction

The LIN protocol as proposed is an automotive focused low-speed universal asynchronous receiver transmitter (UART)-based network. Some of the key characteristics of the Local Interconnect Network (LIN) protocol are signal-based communication, schedule table-based frame transfer, master/slave communication with error detection, node configuration and diagnostic service transportation.

The LIN protocol is for low-cost automotive control applications, for example, door module and air condition systems. It serves as a communication infrastructure for low-speed control applications in vehicles by providing

- signal-based communication to exchange information between applications in different nodes,
- bitrate support from 1 kbit/s to 20 kbit/s,
- deterministic schedule table-based frame communication,
- network management that wakes up and puts the LIN cluster into sleep mode in a controlled manner,
- status management that provides error handling and error signalling,
- transport layer that allows large amount of data to be transported (such as diagnostic services),
- specification of how to handle diagnostic services,
- electrical physical layer specifications,
- node description language describing properties of slave nodes,
- network description file describing behaviour of communication, and
- application programmer's interface.

ISO 17987 (all parts) is based on the open systems interconnection (OSI) basic reference model as specified in ISO/IEC 7498–1 which structures communication systems into seven layers.

The OSI model structures data communication into seven layers called (top down) *application layer* (layer 7), *presentation layer*, *session layer*, *transport layer*, *network layer*, *data link layer* and *physical layer* (layer 1). A subset of these layers is used in ISO 17987 (all parts).

ISO 17987 (all parts) distinguishes between the services provided by a layer to the layer above it and the protocol used by the layer to send a message between the peer entities of that layer. The reason for this distinction is to make the services, especially the application layer services and the transport layer services, reusable also for other types of networks than LIN. In this way, the protocol is hidden from the service user and it is possible to change the protocol if special system requirements demand it.

ISO 17987 (all parts) provides all documents and references required to support the implementation of the requirements related to the following:

- ISO 17987–1: This part provides an overview of the ISO 17987 (all parts) and structure along with the use case definitions and a common set of resources (definitions, references) for use by all subsequent parts.
- ISO 17987–2: This part specifies the requirements related to the transport protocol and the network layer requirements to transport the PDU of a message between LIN nodes.
- ISO 17987–3: This part specifies the requirements for implementations of the LIN protocol on the logical level of abstraction. Hardware related properties are hidden in the defined constraints.
- ISO 17987–4: This part specifies the requirements for implementations of active hardware components which are necessary to interconnect the protocol implementation.

- ISO/TR 17987–5: This part specifies the LIN application programmers interface (API) and the node configuration and identification services. The node configuration and identification services are specified in the API and define how a slave node is configured and how a slave node uses the identification service.
- ISO 17987–6: This part specifies tests to check the conformance of the LIN protocol implementation according to ISO 17987–2 and ISO 17987–3. This comprises tests for the data link layer, the network layer and the transport layer.
- ISO 17987–7: This part specifies tests to check the conformance of the LIN electrical physical layer implementation (logical level of abstraction) according to ISO 17987–4.

Road vehicles — Local Interconnect Network (LIN) —

Part 7:
Electrical Physical Layer (EPL) conformance test specification

1 Scope

This document specifies the conformance test for the electrical physical layer (EPL) of the LIN communications system. It is part of this document to define a test that considers ISO 9646 and ISO 17987–4.

The purpose of this document is to provide a standardized way to verify whether a LIN bus driver is compliant to ISO 17987–4. The primary motivation is to ensure a level of interoperability of LIN bus drivers from different sources in a system environment.

This document provides all the necessary technical information to ensure that test results are consistent even on different test systems, provided that the particular test suite and the test system are compliant to the content of this document.

2 Normative references

The following documents are referred to in text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17987–4:2016, *Road vehicles — Local Interconnect Network (LIN) — Part 4: Electrical Physical Layer (EPL) specification 12V/24V*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions in ISO 17987–4 and ISO 17987–6 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

NOTE This also includes the device classification of ISO 17987–6:2016, 5.6 into class A/B/C for the different ECU and transceiver types.

3.2 Symbols

%	Percentage
µs	Microsecond
C1/2	capacitance

C_{COMMON}	capacitance in the communication line
$C`_{LINE}$	line capacitance
C_{BUS}	total bus capacitance
C_{MASTER}	capacitance of master node
C_{REF}	reference capacitance
C_{RXD}	RXD capacitance (LIN receiver, RXD capacitive load condition)
C_{SLAVE}	capacitance of slave node
$\in$	mathematical symbol: replacement for “is an element of”
d^2V/dt^2	second derivative of Voltage (Volt^2 per second^2)
di/dt	instantaneous rate of current change (amps per second)
D1/2	diode
D_{ser_int}	serial internal diode at transceiver IC
D_{ser_master}	serial master diode
F_{TS}	test system bit rate
I_{BUS}	current into the ECU bus line
I_{BUS_LIM}	current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$ into ECU bus line
$I_{BUS\_NO\_BAT}$	current at ECU bus line when V_{BAT} is disconnected
$I_{BUS\_NO\_GND}$	current at ECU bus line when V_{GND_ECU} is disconnected
$I_{BUS\_PAS\_dom}$	current at ECU bus line when driver off (passive) at dominant LIN-bus-level (12 V LIN devices: $V_{BUS} = 0$ V and $V_{BAT} = 12$ V; 24 V LIN devices: $V_{BUS} = 0$ V and $V_{BAT} = 24$ V)
$I_{BUS\_PAS\_rec}$	current at ECU bus line when driver off (passive) at recessive LIN-bus-level (12 V LIN devices: 8 V < V_{BAT} < 18 V; 8 V < V_{BUS} < 18 V; $V_{BUS} \geq V_{BAT}$; 24 V LIN devices: 16 V < V_{BAT} < 36 V; 16 V < V_{BUS} < 36 V; $V_{BUS} \geq V_{BAT}$)
GND_{Device}	GND of ECU
kΩ	kilo ohm
kbit/s	kilo bit per second
LEN_{BUS}	total length of bus line
LIN_{Bus}	LIN network
ms	millisecond
nF	nano farad
pF	pico farad
pF/m	pico farad per meter (line capacitance)

R1/2	resistor
R_{COMMON}	resistor in the communication line
R_{BUS}	total bus-resistor including all slave and master resistors $R_{\mathrm{BUS}} = R_{\mathrm{Master}}\|\|R_{\mathrm{Slave1}}\|\|R_{\mathrm{Slave2}}\|\|\mathrm{to}\|\|R_{\mathrm{SlaveN}}$
R_{REF}	reference resistor
R_{master}	master resistor
$R_{\mathrm{pull\_up}}$	pull-up resistor
R_{slave}	slave resistor
t_{BFS}	byte field synchronization time
t_{BIT}	basic bit times
t_{EBS}	earliest bit sample time
$t_{\mathrm{rx\_pd}}$	propagation delay of receiver
$t_{\mathrm{rx\_sym}}$	symmetry of receiver propagation delay rising edge propagation delay of receiver
t_{LBS}	latest bit sample time
$t_{\mathrm{rx\_pdf(1)}}$	propagation delay time of receiving node 1 at falling (recessive to dominant) LIN bus edge
$t_{\mathrm{rx\_pdf(2)}}$	propagation delay time of receiving node 2 at falling (recessive to dominant) LIN bus edge
$t_{\mathrm{rx\_pdr(1)}}$	propagation delay time of receiving node 1 at rising (dominant to recessive) LIN bus edge
$t_{\mathrm{rx\_pdr(2)}}$	propagation delay time of receiving node 2 at rising (dominant to recessive) LIN bus edge
t_{SR}	sample window repetition time
$TH_{\mathrm{Dom(max)}}$	maximum dominant threshold of receiving node (volt)
$TH_{\mathrm{Dom(min)}}$	minimum dominant threshold of receiving node (volt)
$TH_{\mathrm{Rec(max)}}$	maximum recessive threshold of receiving node (volt)
$TH_{\mathrm{Rec(min)}}$	minimum recessive threshold of receiving node (volt)
V	voltage
V_{ANODE}	voltage at the anode of the diode
V_{BAT}	voltage across the ECU supply connectors
V_{BATTERY}	voltage across the vehicle battery connectors
$V_{\mathrm{BS1/2}}$	battery shift
V_{BUS}	voltage on the LIN bus
$V_{\mathrm{BUS\_CNT}}$	centre point of receiver threshold
$V_{\mathrm{BUS\_dom}}$	receiver dominant voltage
$V_{\mathrm{BUS\_rec}}$	receiver recessive voltage

$V_{CATHODE}$	voltage at the cathode of the diode
$V_{CC1/2}$	positive power supply voltage (e.g. 5 V)
$V_{D1/2}$	voltage at diode between anode and cathode
V_{Dom}	dominant voltage
$V_{GND1/2}$	ground shift
$V_{GND\_BATTERY}$	battery ground voltage
V_{GND_ECU}	voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$)
V_{HYS}	receiver hysteresis voltage
V_{IUT}	voltage at IUT supply pins
$V_{PS1/2}$	voltage at remote power supply no. 1/no. 2
V_{Rec}	recessive voltage
$V_{SerDiode}$	voltage drop at the serial diodes
V_{Shift_BAT}	battery shift
$V_{Shift\_Difference}$	difference between battery shift and GND shift
V_{Shift_GND}	GND shift
V_{SUP}	voltage at transceiver supply pins
$V_{SUP\_NON\_OP}$	voltage which the device is not destroyed; no guarantee of correct operation
V_{th_dom}	receiver threshold voltage of the recessive to dominant LIN bus edge
V_{th_rec}	receiver threshold voltage of the dominant to recessive LIN bus edge
$\Delta F/F_{Nom}$	deviation from nominal bit rate
τ	time constant
Ω	ohm

3.3 Abbreviated terms

AC	alternate current
API	application programmers interface
ASIC	application specific integrated circuit
BFS	byte field synchronization
DC	direct current
EBS	earliest bit sample
EMC	electromagnetic compatibility

EMI	electromagnetic interference
EPL	electrical physical layer
ESD	electrostatic discharge
GND	ground
IUT	implementation under test
LBS	latest bit sample
Max.	maximum
Min.	minimum
no.	number
OSI	open systems interconnection
PDU	protocol data unit
RC	RC time constant τ ($\tau = C_{BUS} \times R_{BUS}$)
RX	RX pin of the transceiver
RXD	receive data
SBC	system basis chip
SR	sample window repetition
TRX	transceiver
TX	TX pin of the transceiver
TXD	transmit data
Typ	typical
UART	universal asynchronous receiver transmitter

4 Conventions

ISO 17987 (all parts) is based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical layer, data link layer, network and transport protocol and diagnostic services.

5 EPL 12 V LIN devices with RX and TX access

This clause addresses class A and class B devices.

5.1 Test specification overview

5.1.1 Test case organization

The intention of each test case is described at first, with a short textual explanation. Before tests are executed, the test system shall be set to its initial state as described in 5.2.

The test procedure and the expected results are described in the form of a chart for each test case. Table 1 is a typical test description and defines the test case organization.

Table 1 — Test case organization

IUT node as	Class A/B/C device as master or slave or both	Corresponding test number TC x, TC y, where x, y are the test case number
Initial state	**Parameters:**	
	Number of nodes	Number of node in the test implementation
	Bus loads	In order to simulate a LIN network
	Operational conditions:	
	IUT mode	Operation mode for the IUT (e.g. normal mode, low power mode, ...).
	TX signal	State of TX pin at the beginning of the test.
	RX signal	Logical output voltages of the Rx pin corresponding to recessive/dominant level at the LIN pin are taken from the datasheet of the IUT.
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Value in volt
	Failure	In order to set failure at
	GND Shift	Value in volt
Test steps	Describe the test stages.	
Response	Describe the result expected in order to decide if the test passed or failed.	
Reference	Corresponding number in ISO 17987-4.	

IUT may be a master or slave ECU or an individual transceiver chip. The RX, TX and V_{SUP} signals shall be accessible for proper test execution. It is recommended to test with RX/TX access, if not possible, testing according the specification without RX/TX access (see Clause 6) is accepted. Depending on the type of IUT, the supply voltage is V_{BAT} for ECU or V_{SUP} for a chip, referred to as V_{IUT} in this description.

5.1.2 Measurement and signal generation requirements

Table 2 defines the requirements in measurement and signal generation.

Table 2 — Measurement and signal generation requirements

Signal generation:	Rise/Fall time		<20 ns (square wave) <40 ns (triangle)
	Frequency		20 ppm
	Jitter		<25 ns
Signal measurement:	Dynamic signals:		Oscilloscope 100 MHz rise time ≤3,5 ns
	Static signals:	DC voltage	0,5 %
		DC current	0,6 %
		Resistance	0,5 %
Power Supply (V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS})	Resolution		10 mV/1 mA
	Accuracy		0,2 % of value

5.2 Operational conditions — Calibration

5.2.1 Electrical input/output, LIN protocol

The initial configuration for each test case is defined here. Any requirements for individual tests are specified with the test case.

Table 3 defines the initial state of electrical input/output.

Table 3 — Initial state of electrical input/output

Initial state	**Parameters:**	
	Number of nodes	1
	Bus loads	—
	Operational conditions:	
	IUT mode	Set to normal/active mode
	TX signal	Recessive
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Specified for each test
	Failure	No failure
	GND shift	0 V

5.2.2 [EPL–CT 1] Operating voltage range

This test shall ensure the correct operation in the valid supply voltage ranges, by correct reception of dominant bits. The IUT is therefore supplied with an increasing/decreasing voltage ramp.

Figure 1 shows the test configuration of the test system “Operating voltage range with RX and TX access”.

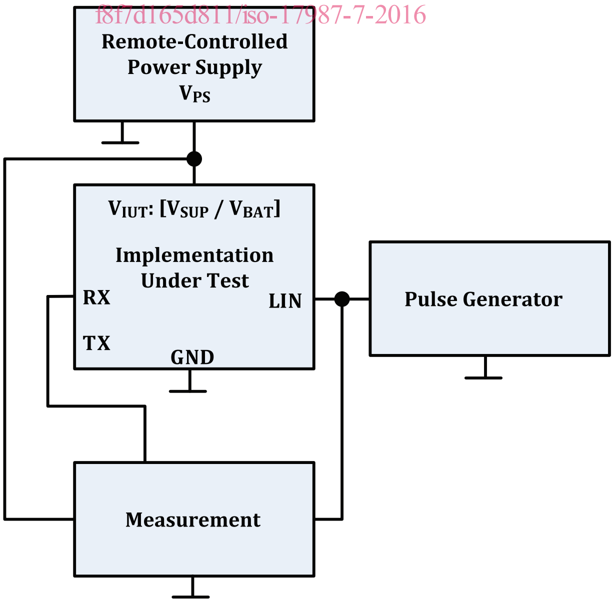

Figure 1 — Test system: Operating voltage range with RX and TX access

Table 4 defines the test system “Operating voltage range with RX and TX access”.