SLOVENSKI STANDARD
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01-september-2002

Sectional specification: Digital monolithic integrated circuits

Sectional Specification: Digital monolithic integrated circuits

Rahmenspezifikation: Digitale monolithische integrierte Schaltungen

Spécification intermédiaire: Circuits intégrés digitaux monolithiques

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Ta slovenski standard je istoveten z: EN 190100:1993

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31.200	Integrirana vezja, mikroelektronika	Integrated circuits. Microelectronics

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2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

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EN 190100

April 1993

Supersedes CECC 90100 Issue 3:1986

Descriptors: Quality, electronic components, integrated circuits

English version

Sectional Specification: Digital monolithic integrated circuits

Spécification intermédiaire: Circuits intégrés digitaux monolithiques

Rahmenspezifikation: Digitale monolithische integrierte Schaltungen

This European Standard was approved by CENELEC Electronic Components Committee (CECC) on 21 January 1993. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the General Secretariat of the CECC or to any CENELEC member.

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This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CECC General Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom. The membership of the CECC is identical, with the exception of the national electrotechnical committees of Greece, Iceland and Luxembourg.

CECC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

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Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This European Standard was prepared by CECC WG 9, "*Integrated Circuits*".

The text of the draft based on document CECC 90100 Issue 3:1986 (with A1 and A2) was submitted to the formal vote for conversion to a European Standard; together with the voting report, circulated as document CECC (Secretariat)3284 it was approved by CECC as EN 190100 on 21 January 1993.

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The following dates were fixed:

— latest date of announcement of the EN at national level	(doa)	1993-02-26
— latest date of publication of an identical national standard	(dop)	1993-08-26
— latest date of declaration of national standard's obsolescence		1993-08-26
— latest date of withdrawal of conflicting national standards	(dow)	2003-02-26

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CECC 90100

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

English version

Harmonized System of Quality Assessment for
Electronic Components

SECTIONAL SPECIFICATION:

DIGITAL MONOLITHIC INTEGRATED CIRCUITS

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Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION INTERMEDIAIRE:

CIRCUITS INTEGRES MONOLITHIQUES LOGIQUES

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

RAHMENSPEZIFIKATION:

DIGITALE MONOLITHISCHE NTEGRIERTE SCHALTUNGEN

3 Issue Edition Ausgabe

CECC 90100

1986

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The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for DIGITAL MONOLITHIC INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the system.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.

Preface

This sectional specification (SS) was prepared by CECC WG 9 "Integrated circuits".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission, and in particular on IEC 747: Semiconductor devices — Discrete devices and integrated circuits.

The text of this third issue consists of the text of CECC 90100 Issue 2 (1983) amended in accordance with the ratified new material introduced by the documents listed below, and was ratified by the President of the CECC for printing as a CECC Specification.

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Document	Date of Voting	Report of Voting	Affected Clause
CECC(Secretariat)1386	July 1983	CECC(Secretariat)1496	3.1
CECC(Secretariat)1571	June 1984	CECC(Secretariat)1678 CECC (Secretariat) 1678A	
CECC(Secretariat)1387	July 1983	CECC (Secretariat) 1497	4.1.3
CECC(Secretariat)1135	November 1981	CECC (Secretariat) 1189	4.1.10
CECC(Secretariat)1269	December 1982	CECC(Secretariat)1339	
CECC(Secretariat)1457	November 1983	CECC(Secretariat)1553	4.2.2
CECC(Secretariat)1127	October 1981	CECC(Secretariat)1172	
CECC(Secretariat)1284	January 1983	CECC(Secretariat)1363	5.3.9
CECC(Secretariat)1186	April 1982		5.4
CECC(Secretariat)1186A	May 1982	CECC(Secretariat)1272	
CECC(Secretariat)1388	July 1983	CECC(Secretariat)1494	
CECC(Secretariat)1389	July 1983	CECC(Secretariat)1495	
CECC(Secretariat)1560	May 1984	CECC(Secretariat)1657	
CECC(Secretariat)1561	May 1984	CECC(Secretariat)1652	

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The text is published initially in French and English. The German version will follow as soon as it has been prepared.

Effective date

This Issue 3 shall become effective for all new applications for qualification approval from 1 June 1986. For current qualifications a transition time of 18 months may be applied. Issue 1 and Issue 2 shall remain valid for existing qualification approval until further notice.

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1 Scope

This specification applies to digital monolithic integrated circuits and shall be read in conjunction with CECC 90000.

It defines methods for:

- — structural similarity
- — electrical measurements
- — electrical endurance measurements

The common blank detail specification (BDS), contained in this SS, comprises those requirements which are common for all digital circuits.

2 General

2.1 Related documents

In each case the latest issue of the document prior to the date of issue of this document is valid.

IEC 148, *Letter symbols for semiconductor devices and integrated microcircuits (Chapter X).*

IEC 617, *Graphical symbols for diagrams.*

IEC 617-12, Part 12: *Binary logic elements.*

IEC 747, *Semiconductor devices — Discrete devices and integrated circuits.*

IEC 747-1, Part 1: *General.*

IEC 747-10, Part 10: *Generic specification for discrete devices and integrated circuits.*

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IEC 748, *Semiconductor devices — integrated circuits.*

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IEC 748-1, Part 1: *General.*

IEC 748-2, Part 2: *Digital integrated circuits.*

CECC 90000, *GS for monolithic integrated circuits.*

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2.2 Preferred voltages for digital monolithic integrated circuits

Preferred values are:

- — bipolar (other than ECL): 1,5; 5,0; 12; 15 V
- — ECL: 5,2 V
- — MOS: 1,3; 1,5; 3,0; 5,0; 10; 12; 15; 18; 24 V

2.3 Symbols and terminology

2.3.1 *Terms*

For terminology, IEC 747-1 shall be used, and in particular Section IV.

2.3.2 *Letter symbols*

The letter symbols shall be used in accordance with IEC 148, Chapter X.

To indicate a defined value of an electrical quantity denoted by a basic letter, the following system shall be used:

- — A for the most positive (least negative) value of the range
- — B for the least positive (most negative) value of the range.

For digital variables the following notations may be used:

- — that range which is closest to positive infinity is to be called the “H” range
- — that range which is closest to negative infinity is to be called the “L” range
- — that boundary of any range which is closest to positive infinity is to be called the “A” value
- — that boundary of any range which is closest to negative infinity is to be called the “B” value.

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Examples (see Figure 1).

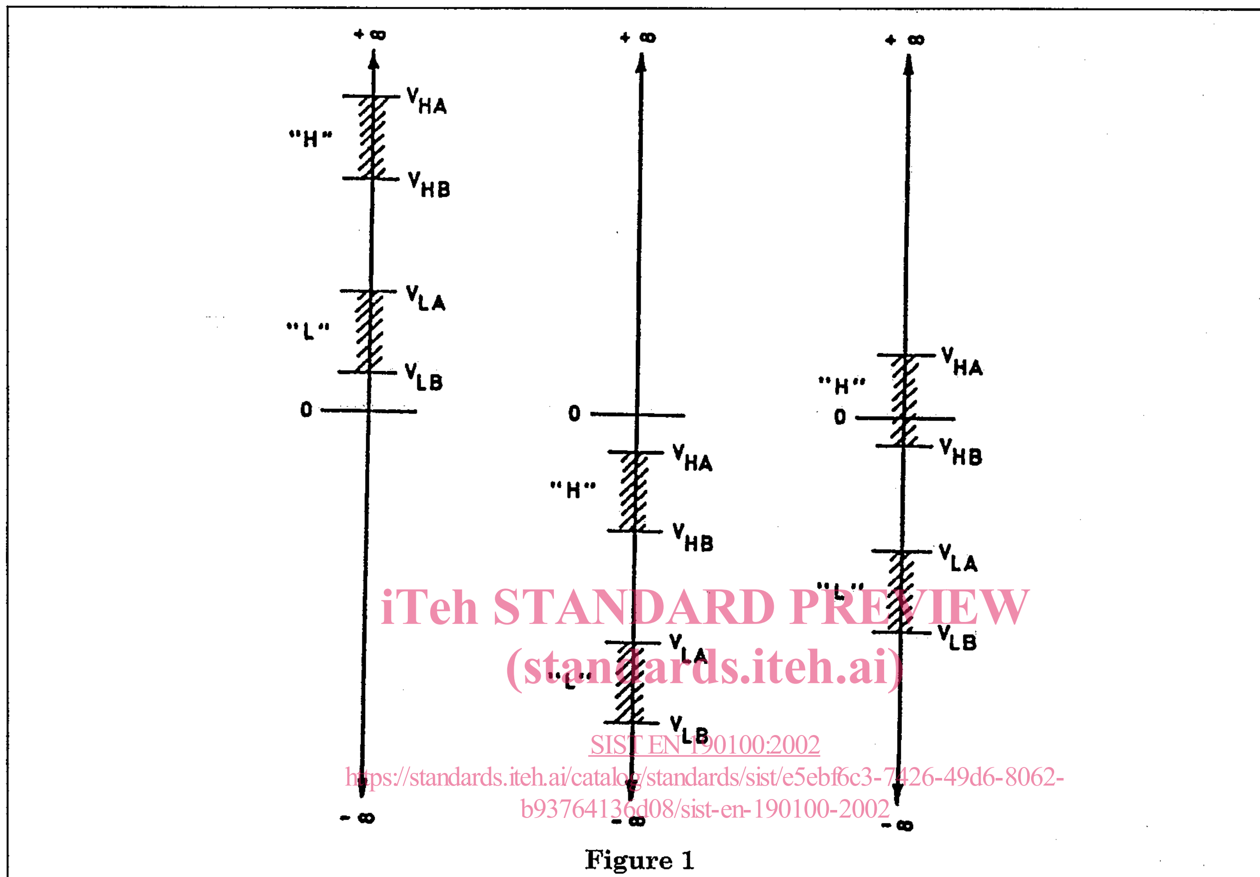

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Figure 1

2.3.3 ***Graphical symbols***

Graphical symbols shall be used in accordance with IEC 617-12.

3 Quality assessment procedures

3.1 Structurally similar circuits (see **3.2** of CECC 90000)

The grouping of types due to structural similarity is as follows:

3.1.1 For testing of Sub-Groups B1 — Dimensions
C1 — Dimensions (not included in B1)

the devices are structurally similar provided that they have identical packages, and that they come from the same assembly and encapsulation line using the same assembly techniques and piece parts.

3.1.2 For testing of Sub-Groups B2 — Solderability
B3 — Sealing test (cavity packages)
B4 — Change of temperature
C2 — Immersion in cleaning solvents
C3 — Robustness of terminations
C4 — Resistance to soldering heat followed by change of temperature
C5 — Shock, vibration, acceleration (cavity packages)
C6 — Damp heat, steady state (cavity packages)
C13 — Salt mist

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The devices are structurally similar provided that:

a) all devices have packages identical in construction and differing only in the number of leads. A single group of devices may be formed provided that the difference between the maximum and minimum number of leads of the devices in that group shall be for:

— Max. number of leads $\leqslant$ 24 Difference $\leqslant$ 4

— Max. number of leads $>$ 24 Difference $\leqslant$ 8

b) all devices come from the same assembly and encapsulation line using the same assembly techniques and piece parts.

c) the ratio of maximum to minimum chip area within a single group of devices shall not exceed 2.

3.1.3 For testing of Sub-Groups B5 — Electrical endurance (168 h)
C8 — Electrical endurance (1 000 or 2 000 h)
D1 — Electrical endurance (8 000 h)

the devices are structurally similar provided that:

a) all devices operate at the same recommended operating voltage(s) and the power dissipation shall be less than 1,2 times that of the device which has been tested.

b) all devices have been designed to the same design rules (e.g. current density and electrical field strength).

c) all devices have been manufactured on the same production line using the same technical processes, including assembly, and starting from the primary stage.

d) the chip layout may differ but the devices with the highest recommended operating temperatures shall be chosen.

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3.1.4 For testing of Sub-Groups C9 — Storage, dry heat
C10 — Storage, cold

the devices are structurally similar provided that all devices have been manufactured on the same production line using the same technical processes starting from the primary stage.

3.1.5 For testing of Sub-Group C7 — Damp heat, steady state (non-cavity packages)

the devices are structurally similar provided that:

a) they operate at the same recommended operating voltages

b) they have been designed to the same design rules

c) they have been manufactured on the same production line using the same technical processes starting from the primary stage.

3.1.6 ***For testing of Sub-Group C14 — Transient energy rating***

The devices are structurally similar provided that:

a) they have been designed to the same design rules

b) they have been manufactured on the same production line using the same technical processes starting from the primary stage.

3.1.7 When the conditions under **3.1.1**, **3.1.2**, **3.1.3**, **3.1.4**, **3.1.5** and **3.1.6** apply, the manufacturer may select a single sample of any one type. The type chosen shall be representative for a group of types in relation to a group of tests, may differ from period to period, dependent on the types produced in that period. The type selected for the group of tests shall be represented by the most complex circuit or that with a critical rating, giving the greatest risk of failure in that group of tests. If there is no significant difference in the characteristics being tested the sample shall be chosen on a rotational basis from current production.

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3.2 Certified test records

Certified test records shall give the following information, unless otherwise specified:

— attributes information for tests in Sub-Groups: B2, B3, B4, B5, C3, C4, C5, C6, C7, C8, C9, C10

— measurement information before and after endurance test: C8 and D1.

4 Test and measurement procedures

4.1 Electrical measurement procedures (see 4.1 and 4.5 of CECC 90000)

4.1.1 *Verification of the function*

Purpose: To confirm that the behaviour of a digital integrated circuit is in accordance with the concise description given in the detail specification (DS) and to check absence of interaction between unrelated sections.

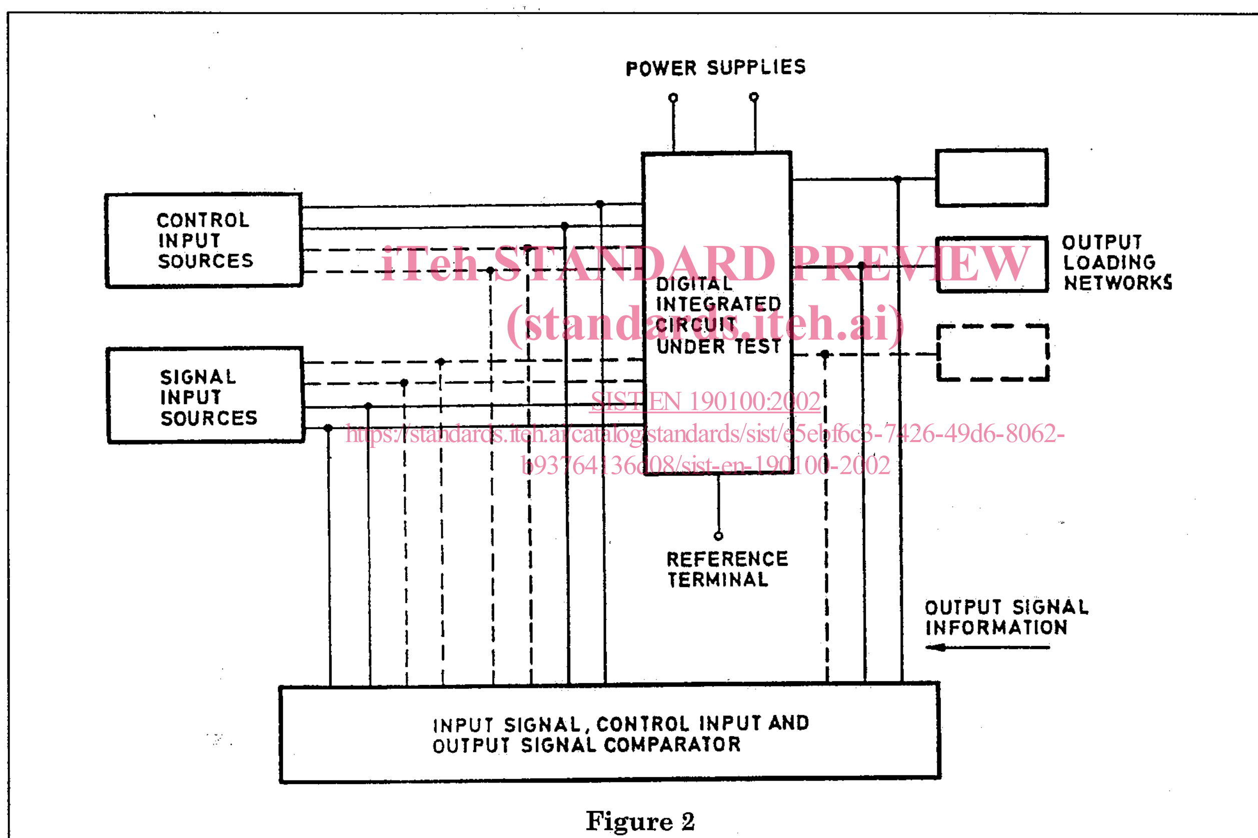

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Figure 2

Description: All inputs (signal and control) shall be operated in accordance with the intended function of the integrated circuit and all resulting output(s) shall be in accordance with that function.

Digital circuits shall be tested in accordance with the specified function table or function matrix at nominal supply voltages, unless otherwise specified. The input, control and output terminal voltages shall be held inside the appropriate specified ranges between V_{OLB} and V_{OLA}, and between V_{OHB} and V_{OHA}. Terminals which are described as having no connections shall be so verified.

Procedure: The temperature conditions shall be 25 °C nominal unless otherwise stated. The digital integrated circuit is inserted into the test socket in accordance with its type designation marking and its terminal identification.

The supply voltages, input and control signals shall be set to their specified values and, where necessary, checked over their ranges and combinations, and the outputs shall comply with the DS.

The voltages and currents shall be reduced to zero and the digital integrated circuit removed from the test socket.

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Specified conditions: The DS shall prescribe:

— supply voltages

— the input, control and output conditions and their inter-relationship both coincidentally and sequentially.

4.1.2 ***Measurement of static characteristics***

It is necessary to test or measure the voltages for each state of the output and to guarantee that these shall be within specified limits when specified voltages are applied to the input terminals and when specified output currents are drawn from, or forced into the output terminals.

The output voltages shall lie between

V_{OHA} and V_{OHB}, and between V_{OLA} and V_{OLB}.

The permitted ranges of the input voltages are between

V_{IHA} and V_{IHB}, and between V_{ILA} and V_{ILB}.

In some technologies the currents associated with the input voltages represent the static input loading requirement of each device and it is necessary to test or measure that the input consumption over the permitted range of input voltages is not outside specified or guaranteed limits. Also, that the currents associated with the output voltages represent the output loading capability of each device. The output loading capability is a specified characteristic.

In the following test methods, the permitted input voltages, output currents or loads are used as test conditions for the measurement of the output voltages. Thus V_{ILA} and I_{OHA} are used for the measurement of V_{OH} for inverting gates and V_{IHB} and I_{OHA} are used for the measurement of V_{OH} for non-inverting gates. Also, the permitted input voltages are used for the measurement of the associated input currents.

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Integrated circuits are designed to operate over a specified range of supply voltages and over a specified range of temperatures. The values of input and output voltages and currents will vary depending upon the supply voltage, the operating temperature and the input and output loadings.

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For acceptance purposes, it is not necessary to test and measure all the possible variations of the static characteristics. There are certain worst case conditions which give an overall limiting set of static characteristics and the testing of these worst case configurations is sufficient.

Standard testing procedure: The following procedure shall be used for all the tests of **4.1.2**.

Procedure: The temperature conditions are set to the specified value and checked before and after the measurement.

The integrated circuit is inserted into the test socket in accordance with its marking and terminal identification.

The supply voltage(s), input voltage(s) and output current or output loading network are set to their specified values and the output voltage is measured.

The voltages and currents are reduced to zero and the digital integrated circuit removed from the test socket.

1) — Low level output voltage (combinatorial circuits)
Purpose: To measure the low level output voltage of a combinatorial digital circuit under specified input voltage, output loading and power supply conditions.

Description: The measurement shall be made under the specified supply voltage conditions. The output loading network shall be adjusted to its specified value or to allow the maximum specified low level output current to flow into or out of the output terminal; a current generator may be used.