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Space systems — Semiconductor integrated circuits for space applications — Design requirements

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ISO copyright office
Ch. de Blandonnet 8 • CP 401
CH-1214 Vernier, Geneva, Switzerland
Tel. +41 22 749 01 11
Fax +41 22 749 09 47
copyright@iso.org
www.iso.org

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

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The committee responsible for this document is ISO/TC 20, *Aircraft and space vehicles*, Subcommittee SC 14, *Space systems and operations*.

Introduction

Normative design requirements of semiconductor integrated circuits for space applications largely determine the reliability of an integrated circuit (IC) and its adaptability to space environment, thereby affecting the reliability of space systems. IC tests and experiments based on product specification only can provide a comprehensive evaluation of its reliability. Once applied to space systems, the design flaws will directly affect the implementation of aerospace engineering. The development of design requirements for semiconductor ICs for space applications can ensure its reliability and space suitability from its very source to meet the space application requirements.

Space systems — Semiconductor integrated circuits for space applications — Design requirements

1 Scope

This document specifies the basic design requirements for semiconductor ICs for space applications, including its design process, as well as required tasks and requirements of each stage. Requirements of specific circuit design are not included.

2 Normative references

The following documents are referred to in text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-2, *Integrated circuits — Measurement of electromagnetic emissions*

IEC 62132, *Integrated circuits — Measurement of electromagnetic immunity*

IEC 62215-3:2013, *Integrated circuits — Measurement of impulse immunity — Part 3: Non-synchronous transient injection method*

IEEE 1149.1, *IEEE standard for test access port and boundary — Scan architecture*

3 Terms and definitions

For the purposes of this document, the terms defined in ISO 10795 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— IEC Electropedia: available at http://www.electropedia.org/

— ISO Online browsing platform: available at http://www.iso.org/obp

3.1
programmable logic device
PLD
hardware-programmable device

EXAMPLE FPGA, CPLD, etc.

3.2
suitability
degree to which a product meets its requirements

3.3
environment adaptability
ability to achieve the entire product's intended functions, performance and (or) capacity for protecting itself under various environments within its life cycle

3.4
testability
ability to perform function and performance testing of the circuit, position the failure of the circuit and select qualified circuit chip as soon as possible

4 Abbreviated terms

ASIC	application specific integrated circuit
BIST	built-in self test
CMOS	complementary metal oxide semiconductor
DFT	design for test
DRC	design rule checking
EMC	electro-magnetic compatibility
ERC	electrical rule checking
ESD	electrostatic discharge
FPGA	field programmable gate array
IC	integrated circuit
I/O	input/output
IP	intellectual property
JFET	junction field effect transistor
MOSFET	metallic oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
RAM	random access memory
RC	resistance capacitance
ROM	read only memory
RTL	register transfer level
SAR ADC	successive approximation register analogue digital converter
SCR	silicon controlled rectifier
SEL	single event latch-up
SET	single event transient
SEU	single event upset
SOI	silicon on insulator
SOS	silicon on sapphire

5 General requirements

General requirements in designing semiconductor ICs for space applications include:

a) process conducted under a fault-tolerant system with design requirements;

NOTE 1 Special implements are allowed for different types of ICs for space applications.

b) adherence to existing standards and regulations during the design process;

c) feasibility and risk analysis of requirements from aerospace customer to validate the rationality of its functional and performance requirements;

d) conversion of users' requirements into design input, which may involve the following steps:

1) derating the design criteria;

NOTE 2 Derate on the basis of nominal stress according to the stress of the circuit. The key is the level and effects. Derating can improve reliability, but takes into consideration issues such as reliability, size, weight and cost.

2) applying fault-tolerant design and adopting rational use of redundant technology;

3) ensuring the characteristics of the orbit thermal environment for reliable thermal design;

4) considering radiation hardness to ensure grade requirements, if necessary;

5) taking note of the life of customer's requirements (mean time to failure);

e) decomposition of the design input requirements to each design stage according to its tasks.

NOTE 3 Implement and validate each step until all objectives and requirements of a semiconductor IC for space applications are achieved.

6 Design process

6.1 Overview

IC designs generally include architecture design, logic design, circuit design and layout design. In order to ensure the validity of the design, computer simulation and verification of its results at each stage are necessary. Figure 1 illustrates the IC design flow.

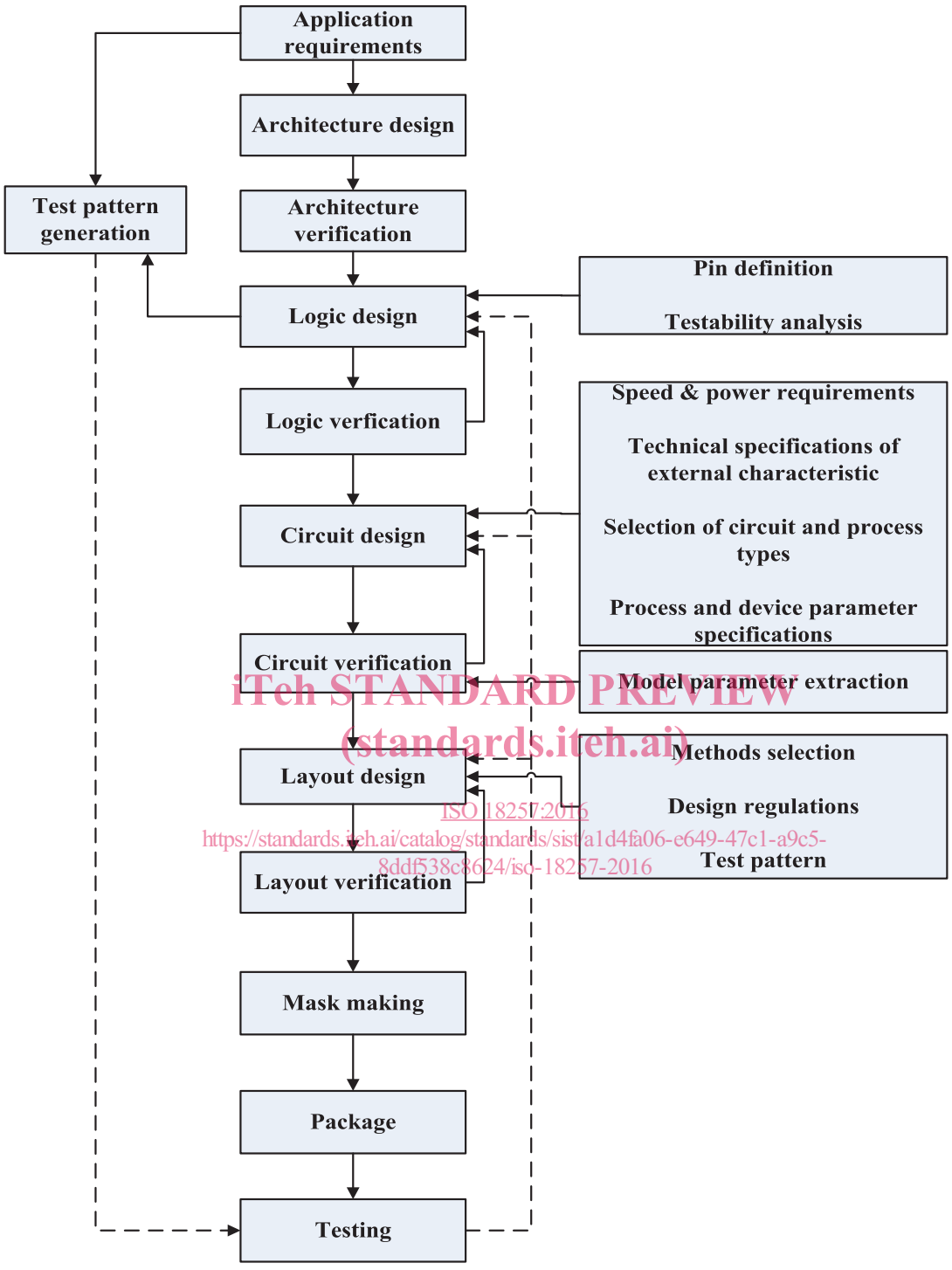

Figure 1 — Integrated circuit design flow diagram

In designing semiconductor ICs for space applications, designers have to follow a general IC design process to convert users' general and special requirements (i.e. user-oriented features, performance and reliability requirements, etc.) into design input, thereby accomplishing the design goals of each stage to meet the overall requirements. Figure 2 illustrates the decomposition of tasks in the design process of semiconductor IC for space applications.

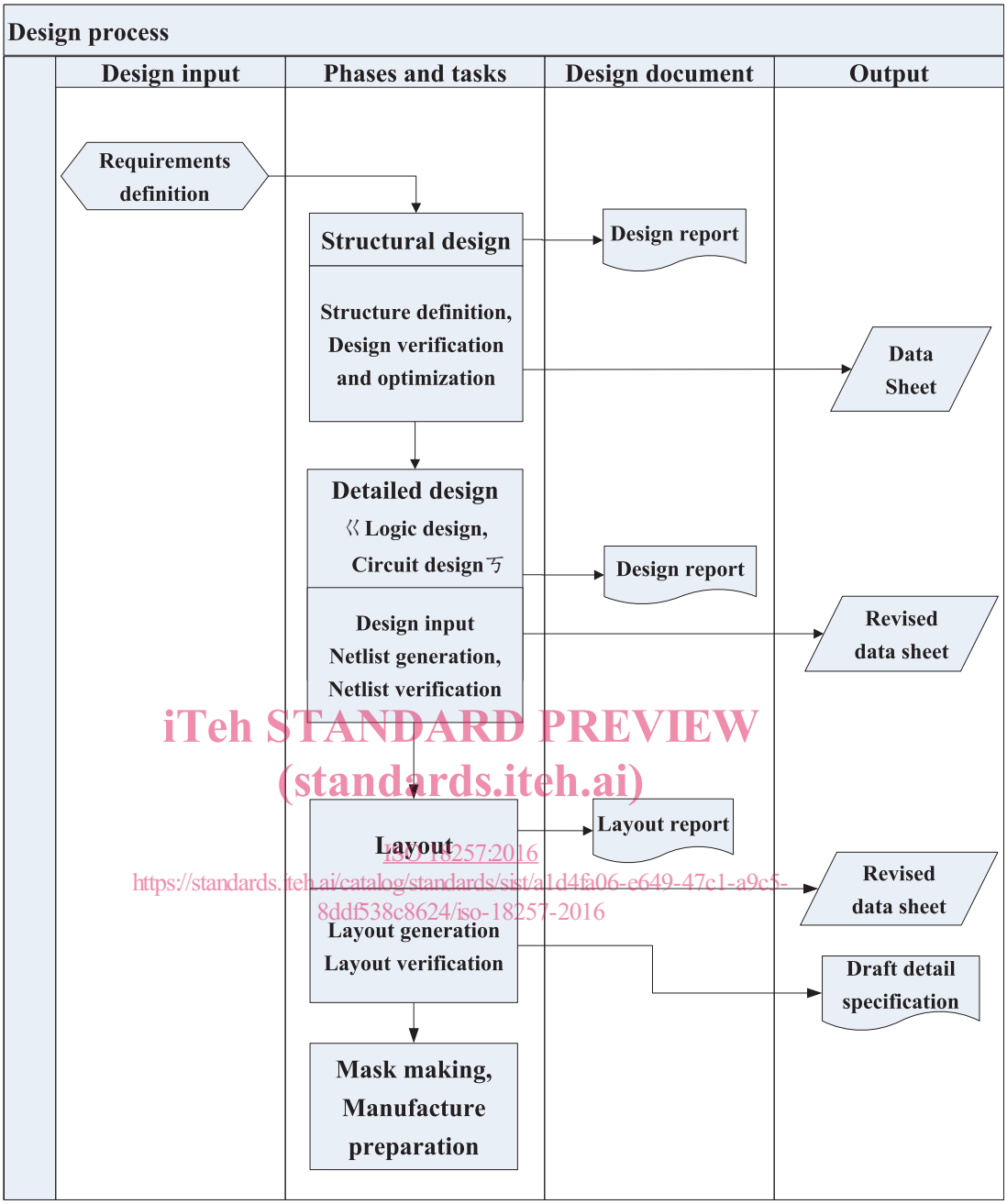

Figure 2 — Decomposition of tasks in designing semiconductor IC for space applications

6.2 Design input

A design input document will be formed after completing the requirements definition. Design input generally includes (modifications are allowed according to specific circuit requirements) the following:

a) system division, system configuration and operating mode;

b) system interface, external device communication protocols, including memory-mapped register;

c) operating frequency range;

d) constraints of electrical parameter;

e) functional requirements;

f) application algorithm;

g) reset and power dissipation requirements;

h) error handling;

i) testing mode;

j) fault coverage requirements of digital circuit testing;

k) key signal timing;

l) constraints of the normal working environment;

m) constraints of the special space working environment, which includes

   1) space radiation,

   2) heat dissipation in vacuum, and

   3) in-space charging effects (i.e. ESD, latch-up);

n) power dissipation budget;

o) physical and mechanical constraints include: pin distribution, size, packaging;

p) reusability and additional features of the product;

q) new technologies;

r) intellectual property of design;

s) IP cores that are necessary and with verification.

6.3 Design phases and tasks

6.3.1 Architecture design

6.3.1.1 Overview

Finding an architecture design that offers efficient functionality at minimal cost, while meeting users' objectives and constraints, is important.

6.3.1.2 Design content

The following is the architecture design process.

a) Define the chip architecture, verify and record the completion of functions of the basic module, as well as interfaces and interactions.

b) Select and validate the chip architecture.

c) Ensure that all definitions and selections are in accordance with the documents made in the definition phase.

d) Ensure that the output includes:

   1) a simulation model,

   2) the results verification, and

   3) a preliminary datasheet.

