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Description of the reliability test structures of the European mini test chip

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This European Prestandard has been prepared by CENELEC Technical Committee TC 217, Electronic Design Automation.

The text of the draft was submitted to the CENELEC members for comments and was approved as ENV 50219 during the CLC/TC 217 meeting on 1995-10-16.

The following date was fixed:

- latest date by which the existence of the ENV has to be announced at national level (doa) 1996-04-01

Contents

1 Introduction

This document is part of a series of documents describing a technology assessment system cycle of submicron CMOS technologies. The series consists of eight closely related documents [1, 2, 3, 4, 5, 6, 7, 8] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle[1] is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS techologies down to 0.5 µm is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in [3]. The documentation of the measurements of these test structures is the objective of [4]. The document [5] contains the techniques used for the extraction of transistor model parameters. The purpose of document [6] is the presentation of a data exchange format which can be used with existing data evaluation programs. Test structures for a fast reliability assessment with respect to the major failure mechanisms in CMOS technologies are described in this document. The measurements required for the characterization of the reliability test structures are documented in [7]. The evaluation of these measurements is subject of document [8].

This publication documents the parametrized test structures of the JESSI **Reliability Test Chip** (RTC) which is part of the **European Mini Test Chip** (ETC). The modules of the ETC provide a minimum set of test structures to characterize a technology between 0.5 µm and 2 µm. The test structures of the ETC are generated automatically by a computer program for a given MOS technology.

The development of the test structures of the European Mini Test Chip is part of the Joint European Submicron Silicon Initiative JESSI AC 41 consortium[2]. They are developed in cooperation with the participants of the JESSI Joint Logic Project (JLP) and JESSI AC41 Technology Assessment consortium. The usefulness of the reliability test structures RTC documented here were verified by means of three different JESSI test chips. The European Mini Test Chip is processed with at least five different CMOS technologies and one BiCMOS technology of the JESSI AC 41 and Joint Logic projects. The minimum feature sizes of the CMOS technologies range from 0.8 µm down to 0.5 µm. Additionally, the test structures were implemented into in-house chips which are not part of the JESSI projects. Consequently, the base of the verification of the test structures is even wider than the number of JESSI test chips indicates.

For the next generation of technologies (0.35 µm and less) the validity of them has to be proven and eventually adapted . The basic test structures described in this document mainly aim as test vehicles to obtain early results on failure mechanisms even in non-mature semiconductor technologies. In-depth reliability evaluation, for e.g. qualification purposes, may require additional structures.

[1] The Technology Assessment Support Center (TASC) provides detailed information about the computer programs which support the measurements and extraction routines. Send a fax or email to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart. Fax: +49-711-685-5930. Email: tasc@svlsi.mikro.uni-stuttgart.de

[2] This work is part of the JESSI Project AC 41 "Technology Assessment" and is sponsored by the national Public Authorities of Belgium, France and Germany

1.1 Scope

The purpose of the reliability test chip RTC is to provide a minimum set of test structures for a fast reliability assessment of emerging CMOS technologies down to 0.5 µm.The basic test structures described in this document are used as test vehicles to obtain information about failure mechanisms even in non-mature semiconductor technologies.

The failure mechanisms which are addressed by the RTC are the following:

1- latch up
2- hot carrier degradation of transistors
3- time dependent dielectric breakdown of thin oxides
4- electromigration in metal lines and contacts

The number of test samples and the failure criteria will depend on the purpose of the tests. Guidelines are given in [8].

1.2 General remarks

The test structures described here are suitable for technologies up to three metal layers. The test structures must have experienced all process steps including the final passivation to ensure all possible influences of different process steps (e.g. temperature profiles, radiation damage) are included. Structures for highly accelerated stress tests are included as well as conventional reliability structures to determine lifetimes by means of common reliability models. Results can also be used to compare them with reliability simulations which are of increasing importance for submicron technologies.

2 Basic modules

The modular concept of the RTC gives the possibility to arrange subsets of the modules within Process Control Monitors (PCM) and other supplier specific test chips. The test structures of the RTC can be used as scribe lane inserts by replacing the standard pad group of the RTC (see 2.1) by a special pad arrangement to meet the actual width of the scibe lane.

The test structures of the modules of the RTC are implemented into a CAD (Computer Aided Design) tool. This program is named Parametric Test structure Generator system (PTG)[1]. By means of the PTG program the test structures are automatically generated for different CMOS processes and different technology generations. The CAD program generates the test structures including the connections to the standard pad group by means of a rule file which contains the design rules of the given CMOS technology. The test structures generated this way can be included in any test chips. In addition, the test structures can be utilized for scribe lane inserts. The standard pad group has to be replaced by a special pad group which is adapted for the use with scribe lanes.

The test structures of the RTC are placed into 9 modules. These modules form the entire RTC and they are named RLUPA, RLUPB, RNMOS, RPMOS, ROXID, RCONS, RCONC, RSWET and RNIST (R stands for reliability), according to the naming convention for standard basic modules used within the JESSI AC 41 consortium. The reliability relevant dimensions of the modules have been fully parameterized (e.g. length of transistors). In other cases the size of the test structures has been optimized for an actual failure mechanism and dimensional restrictions of the module (e.g. area of capacitors). The actual dimensions of such structures can be obtained from the documentation file which is generated by the PTG program. This file shows the geometries of the test structures realized by a given technology.

[1] User's manual ptc-gen rtc-gen Version 2.2 February 1995, IMS Stuttgart

2.1 Minimum standard module and pad group

A minimum size standard module is built up with the pad group shown in figure 1. The test structures are placed in the frame provided by the standard module. Outside the module, at the upperleft corner the name of the module is placed. The name consists of five characters. The frame for the module is located around the pad group keeping a distance of 25 µm from the pads. An edge sensor (ES) is placed outside the frame at the right side of the module. The edge sensor is made of a metal bar. This sensor is used by some measurement systems which probe by means of needle cards and an edge sensor switch. The configuration of the module causes a total size of the modules of 2000 µm x 400 µm. The name of each module is designed using the highest level of metal. Therefore, the name of the module can be identified even on a chip with many metal layes and planarization layers. Table 1 shows the properties of the basic module.

Table 1: Basic module properties

module name:	reliability related modules have names with five characters the name is printed by use of the highest level of metal.
origin:	"O" in the lower left corner of the module
size:	2000 µm x 400 µm
edge sensor:	a vertical metal bar on the right side of the module
padgroup:	the pads are arranged in two rows with pitches of 200 µm in a row and 200 µm between the rows
pad shape:	octagonal
pad size:	100 µm x 100 µm
metal area:	8437 μm^2
passivation window:	90 µm x 90 µm (octagonal)
numbering:	counter clock wise starting at the lower left corner like a dual-in-line package

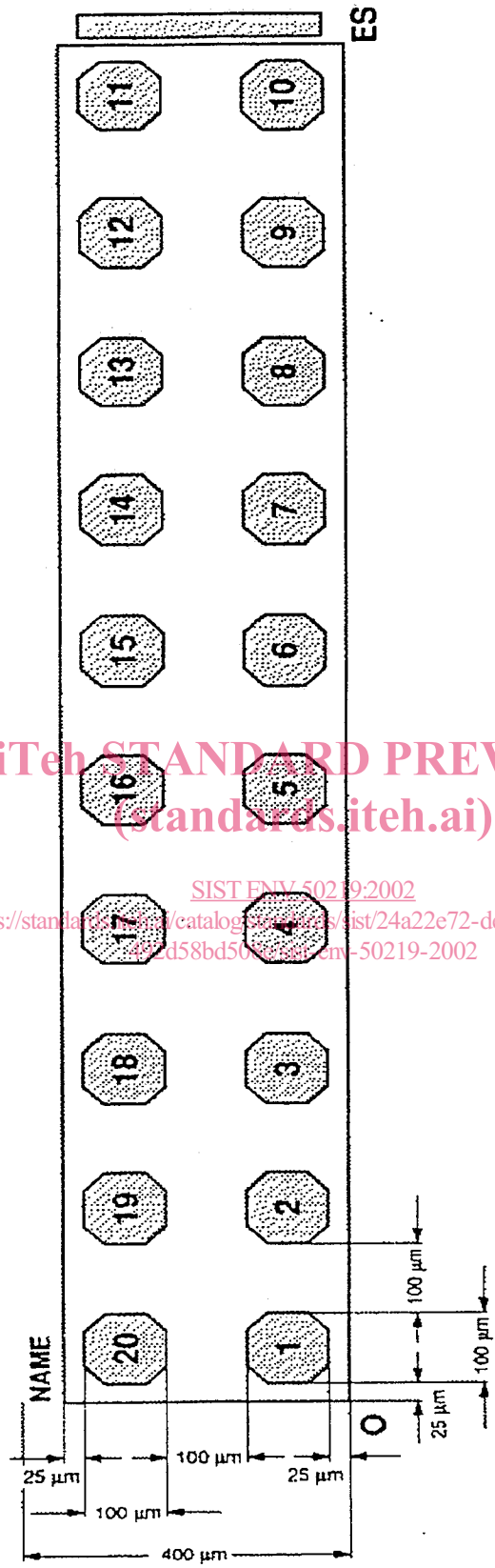

Figure 1: Standard pad group of all modules

2.2 Parameterization of Test Structures

To apply test structures to different technologies it is necessary to describe them in a general way and adjust them afterwards to a certain technology. This is obvious e.g. for the minimum drawn transistor Length (L_{min}) but also other parameters given by the design rules which vary from technology to technology. Table 2 shows an overview how many parameters will be adjusted automatically using PTG and how many will be held constant for a specific technology.

Table 2: Overview of test structures (see detailed descriptions in text and annex 1))

Name of test module	Design rule dependent	Fixed parameters	User defined parameters
RLUPA	d_{min}, $d_{nact,pact}$ W_{act}	L_{act} = 50 µm	
RLUPB	$d_{nact,pact}$, $d_{nact,strap}$ W_{act}	L_{act} = 50 µm $pwell_1$,nact = 60 µm $pwell_2$,nact = 30 µm $d_{pact,nstrap}$ = 12 µm	
RNMOS	L_{min}, W_{box}		W_{usen9}, W_{usep9}
RPMOS	L_{min}, W_{box}		W_{usen9}, W_{usep9}
ROXID	area, perimeter	W, L = 20 µm	
RNIST	metalx width *)	Length: 600 squares	
RSWET	metalx width *)	20 units	
RCONS	4 contact sizes		
RCONC	4 contact sizes	10 contacts	

*) x: layers 1,2 and 3

Using the parameterization strategy the sizes are adapted to special needs of every test structure to be measured and evaluated for each technology.

RLUPA

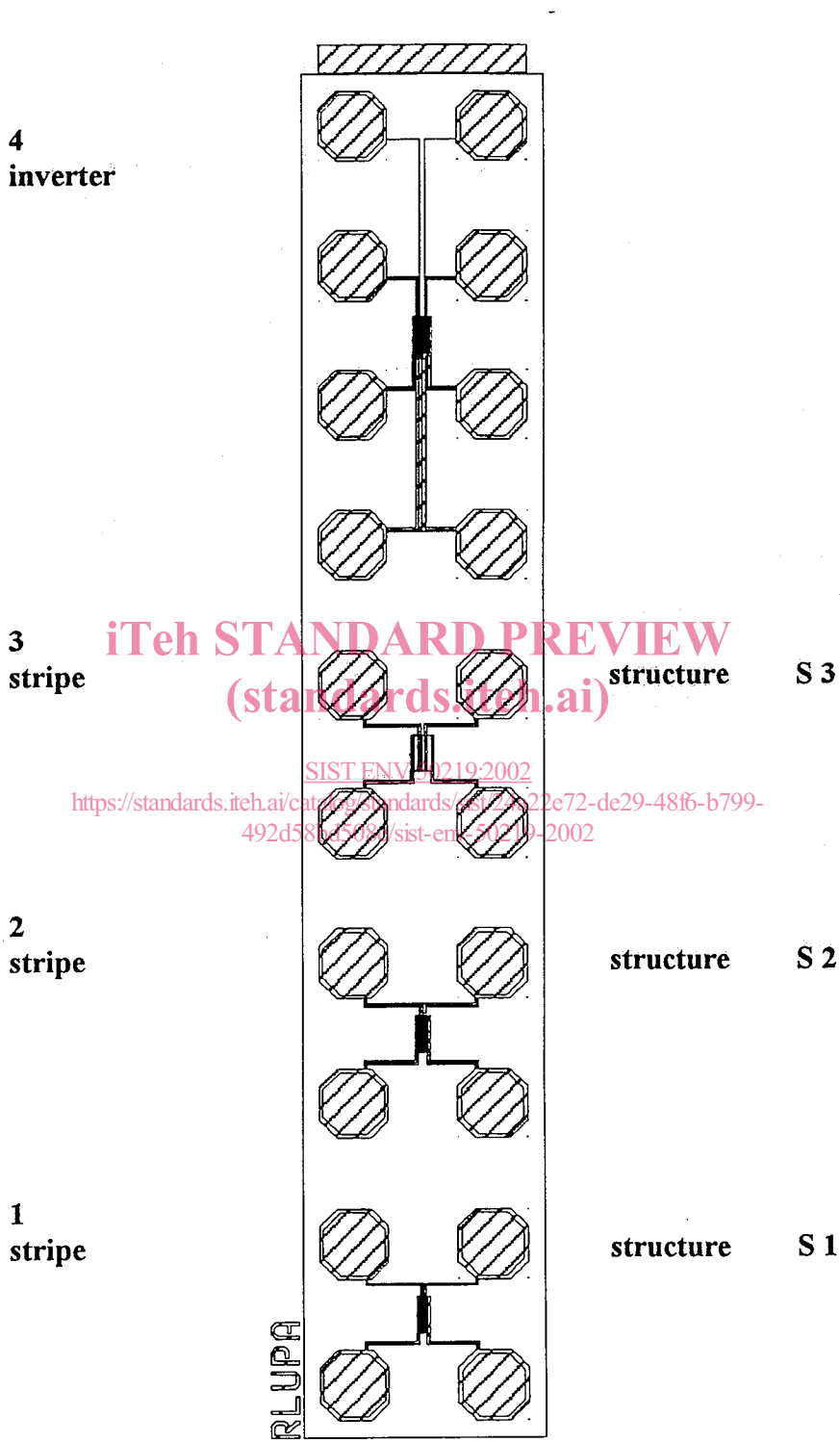

Figure 2: Module RLUPA