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Measurement techniques of the reliability test structures of the European mini test chip

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CENELEC

# R217-010

REPORT

November 1996

English version

# Measurement techniques of the reliability test structures of the European mini test chip

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved by TC 217 on 1996-01-30 and endorsed by the CENELEC Technical Board on 1996-07-02.

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**Foreword**

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# Contents

1 Introduction 4

2 Latch-Up 5

2.1 Introduction 5
2.2 Test structures 7
2.3 Definitions 9
2.4 Test method 10

3 Hot carrier degradation of MOSFETs 14

3.1 Introduction 14
3.2 Test structures 14
3.3 Definitions 14
3.4 Test method for nMOS transistors 16
3.5 Test method for pMOS transistors 20
3.6 Precautions 21

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4 Oxide reliability 22

4.1 Introduction 22
4.2 Test vehicles and structures 22
4.3 Test method 24

5 Electromigration 26

5.1 Introduction 26
5.2 Traditional accelerated stress testing 26
5.3 Fast test methods for comparative purposes 31

Annex A: List of abbreviations 40

Annex B: References 42

# 1 Introduction

This document is part of a series of documents describing a technology assessment system cycle of submicron CMOS technologies. The series consists of eight closely related documents [1, 2, 3, 4, 5, 6, 7, 8] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle[1] is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS techologies down to 0.5 µm is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in [3]. The documentation of the measurements of these test structures is the objective of [4]. The document [5] contains the techniques used for the extraction of transistor model parameters. The purpose of document [6] is the presentation of a data exchange format which can be used with existing data evaluation programs. Test structures for a fast reliability assessment with respect to the major failure mechanisms in CMOS technologies are described in [7]. The measurement techniques required for the characterization of the reliability test structures are documented in this report. The evaluation of these measurements is subject of document [8].

This paper together with [7] and [8] is dedicated to the reliability assessment of a submicron technology. The measurement techniques described here can be applied to any relevant test structure available but they are especially related to the test structures implemented in the reliability test structures of the European Mini Test Chip (ETC).

The development of the test structures of the European Mini Test Chip is part of the Joint European Submicron Silicon Initiative JESSI project AC 41. They are developed in cooperation with the participants of the JESSI Joint Logic Project (JLP) and JESSI AC41 Technology Assessment consortium[2)]. The usefulness of the Reliability Test Structures (RTC) documented here was verified by means of three different JESSI test chips. The minimum feature sizes of the CMOS technologies range from 0.8 µm down to 0.5 µm.

The validity of the test structures as well as the measurement and evaluation techniques has to be proven for the next generation of technologies (0.35 µm and less) and eventually adapted . The basic test structures mainly serve as test vehicles to obtain early results on failure mechanisms even in non-mature semiconductor technologies. In-depth reliability evaluation, for e.g. qualification purposes, may require additional structures and measurement techniques. In general, tests described here are accelerated tests which require an appropriate model which allows to extrapolate to normal operating conditions.

Measurement techniques for the dominant failure mechanisms in submicrometer technologies

- **Latch-up**
- **Hot carrier**
- **Oxide integrity**
- **Electromigration**

are described in detail.

Results gained based on this paper and [8] are well suited to compare technologies. It is not intended to estimate product reliability because this is also very much dependent on the individual design of a product. Therefore product reliability has to be checked for a certain application. Also failure criteria given in this paper are mostly arbitrarily chosen and have to be adapted to a certain application.

[1] The Technology Assessment Support Center (TASC) provides detailed information about the computer programs which support the measurements and extraction routines. Send a fax or email to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart. Fax: +49-711-685-5930. Email: tasc@svlsi.mikro.uni-stuttgart.de

[2] This work is part of the JESSI Project AC 41 "Technology Assessment" and is sponsored by the national Public Authorities of Belgium, France and Germany

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# 2 Latch-up

## 2.1 Introduction

The potential for latch-up exists especially in all bulk CMOS integrated circuits because of the existence of parasitic pnpn paths in these structures. In CMOS inverter structures, for example, the pnpn path runs from the $p^+$ source of the pMOS transistor, through the n-well, into the p-well or substrate and ends at the $n^+$ source of the nMOS. In its simplest form the equivalent circuit consists of a pnp transistor coupled with a npn transistor such that the pnp collector sources the base current of the npn transistor while the npn collector sinks the base current of the pnp transistor (figure 1).
There are also important parasitic resistances, such as the substrate and well resistances, and the emitter resistances of the parasitic bipolars. These must be included in the equivalent circuit model. A cross section of a CMOS inverter structure, together with a schematic of the parasitic bipolar transistors and resistances involved is shown in figure 2.

Under normal bias conditions the pnpn structure is in the "off" state and both bipolar transistors are reverse biased (see figure 2). For the structure to "latch" three conditions must be met:

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1. the emitter-base junction of both transistors must become forwardly biased so that appreciable minority carrier injection occurs,

2. the npn and pnp transistors form a loop of positive current feedback and regenerative switching may result if sufficient loop gain is present. Therefore the product of the bipolartransistor current gains must be sufficient to allow regeneration,

3. the power supplies connected to the external terminals participating in a latch-up must be capable of sourcing or sinking currents larger than the holding current of the pnpn structure.

There are several possibilities which can cause latch-up. The first condition can arise by lateral currents flowing in the 4-layer structure. These currents can be generated by ionizing radiations such as alpha particles, X-rays or gamma rays. Secondly by an overvoltage stress in the applied terminal voltage ($V_{dd}$-$V_{ss}$) resulting in an avalanche current from the reverse biased n-well/ p-well junction, by hot electron substrate currents from short channel devices, and thirdly by voltage transients on the power supply lines resulting in a displacement current from the n-well/ p-well depletion layer capacitance, and by possible forward biasing of junction diodes (e.g. at input/ output circuits).

The aim of this document is to introduce specific structures and methods for having a quick evaluation of the parasitic bipolar transistors which are, in CMOS integrated circuits, responsible for latch-up. Secondly it is the aim to determine, on wafer level, the sensitivity of the technology with respect to latch-up by measuring trigger as well as holding currents and voltages.

Since latch-up is also very dependent upon the layout, this method does not provide a means to determine the latch-up behaviour of real circuits. This is done by the existing JEDEC specification [9] describing latch-up in CMOS integrated circuits.
Comprehensive treatments of the latch-up phenomen can be found e.g. in [10], [11] and [12].

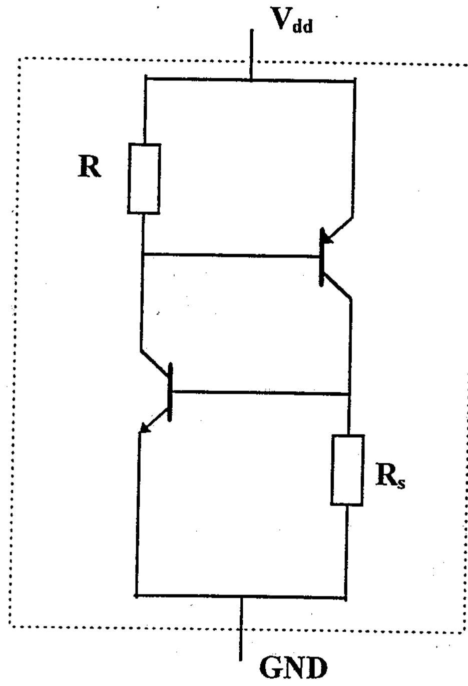


**Figure 1: Simplified circuit for latch-up action in CMOS**

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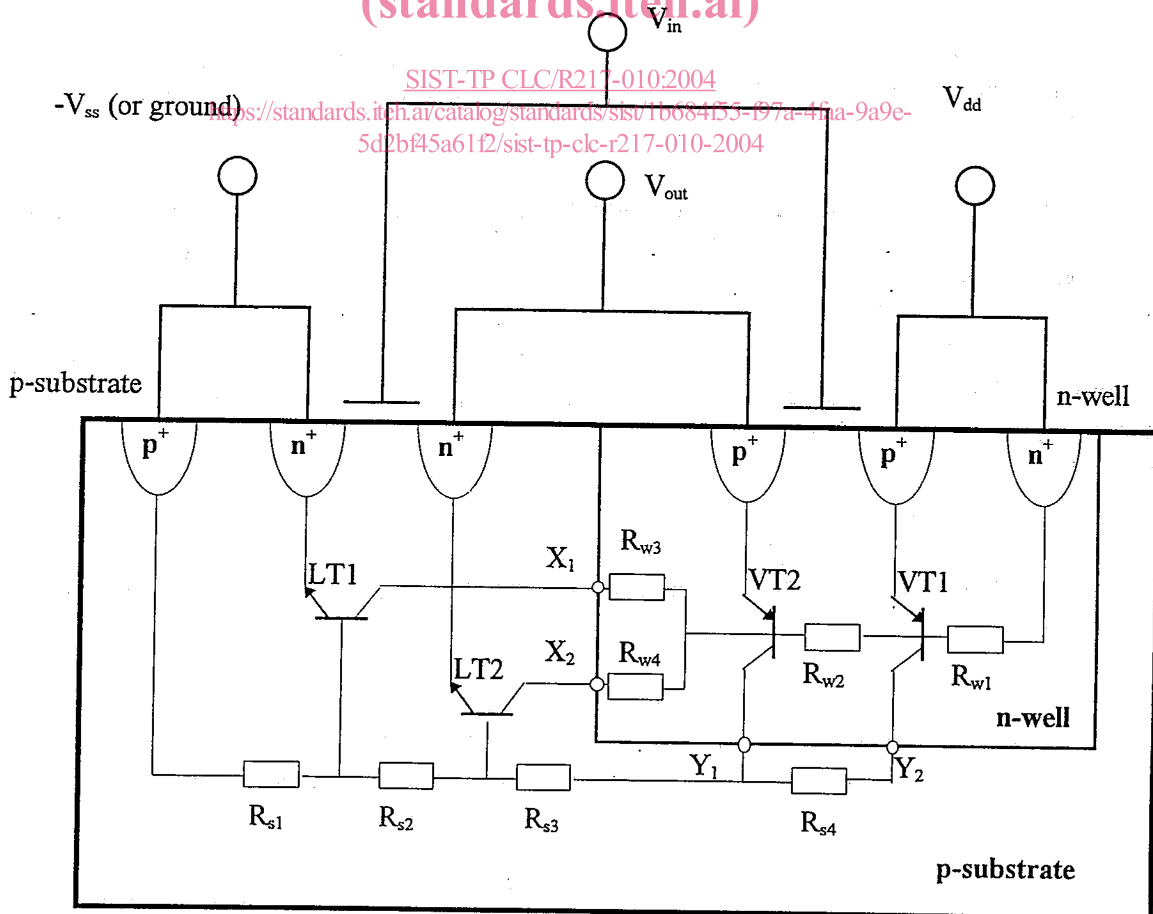


**Figure 2: Parasitic bipolar portion of n-well CMOS inverter after [10]**

## 2.2 Test structures

The test modules RLUPA and RLUPB of the European Mini Test Chip [7] contain test structures to determine the latch-up behaviour of a submicron technology. The module RLUPA has four stripe structures and an inverter-like structure, the module RLUPB contains six stripe structures. The measurement method will be described in detail using the structures of RLUPB.
In figure 3 a cross section of the four stripe arrangement of RLUPA is shown. The width of active areas ($W_{act}$) and the distance of active areas lying in different wells are minimum ($d_{nact,pact}$) based on design rules. The length of the stripes, $L_{act}$ can be defined by the user. This $L_{act}$ corresponds in the inverter-like structure to the width of a transistor. The critical distance between two active areas (in the same well) is the minimum distance given by the design rules ($d_{min}$) and with relaxed design rules ($3*d_{min}$ and $10*d_{min}$). Figure 4 shows the cross section of the inverter-like structure.

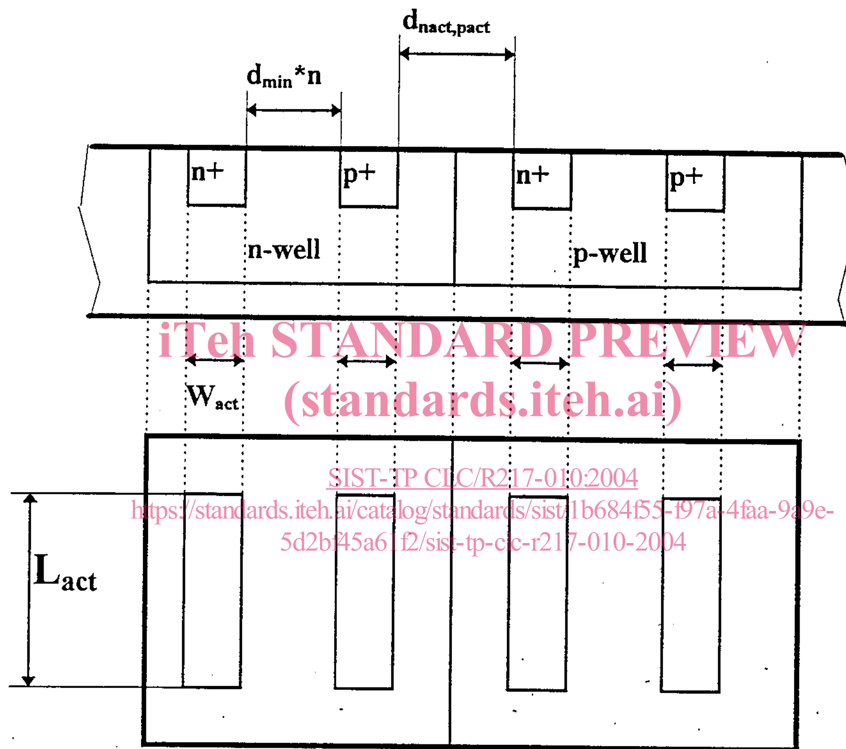


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**Figure 3: Cross section of the four stripe type structure of the RLUPA module, n = 1, 3 and 10**

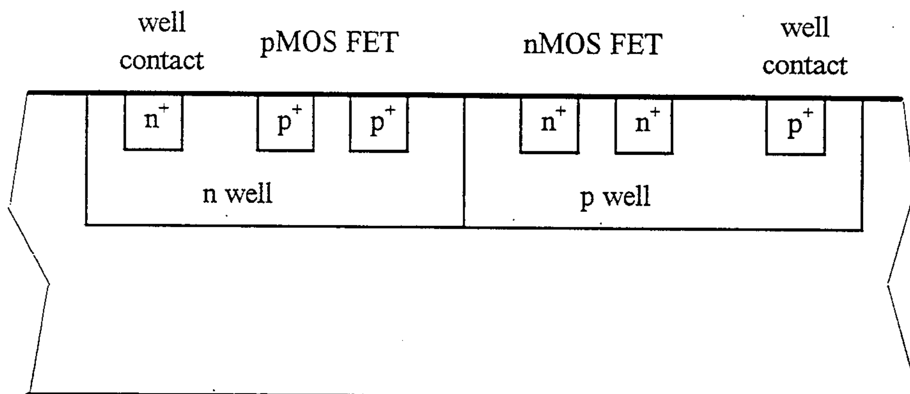


**Figure 4: Cross section of inverter-like structure**

In module RLUPB, two types of latch-up structures are available: type I and type II. The type I structure checks the layout rules for the spacing of different active areas whereas type II is dedicated to the layout rules for the placement of contacts i.e. spacing between similar types of active areas. A layout is shown in figure 5. Type Ia and IIa are designed according to the minimum allowed layout rules, type Ib and IIb are designed with relaxed rules, whereas type Ic and IIc are designed using 90% of the minimum distance between $n^+$ and $p^+$ active. For latch-up comparison purposes, types Ia and IIa should be used. Normally only the layout rules have to be checked, therefore only structures drawn according the nominal layout rules should be measured. This can be done using the structures Ia and IIa. The other structures can be used in the case latch-up occurs to find out whether relaxed rules are sufficient to suppress latch-up and to get an idea how big the margin for latch-up is.

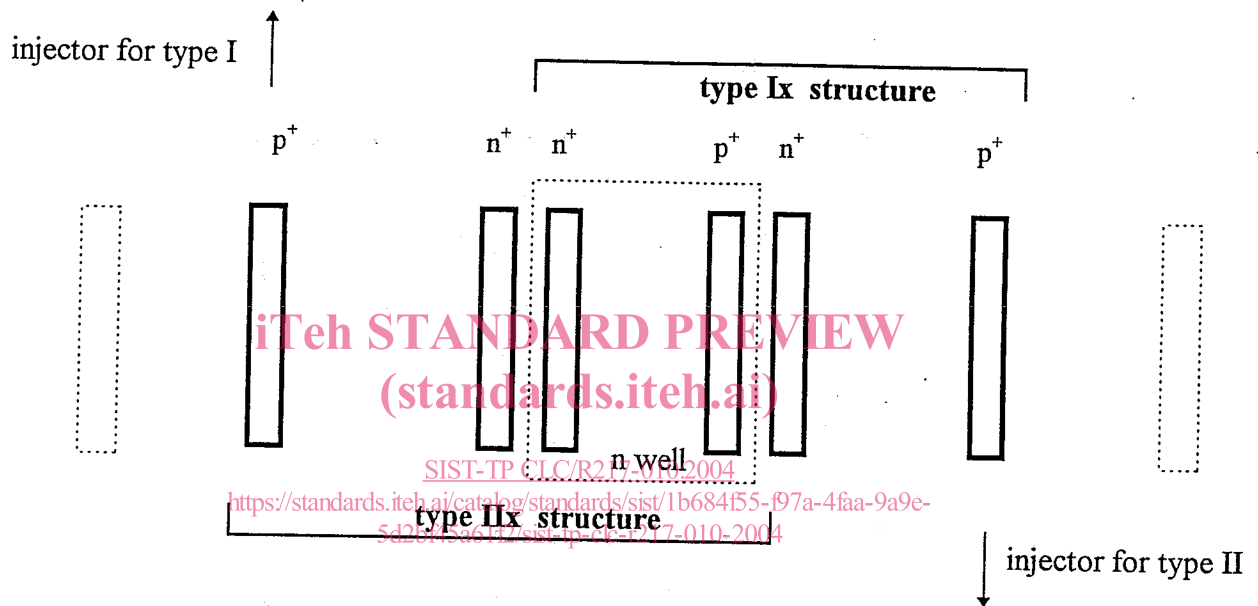


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**Figure 5: Layout of the 6 stripe RLUPB test structure [7], x = a, b or c**

A cross section of the structure is shown in figure 6.

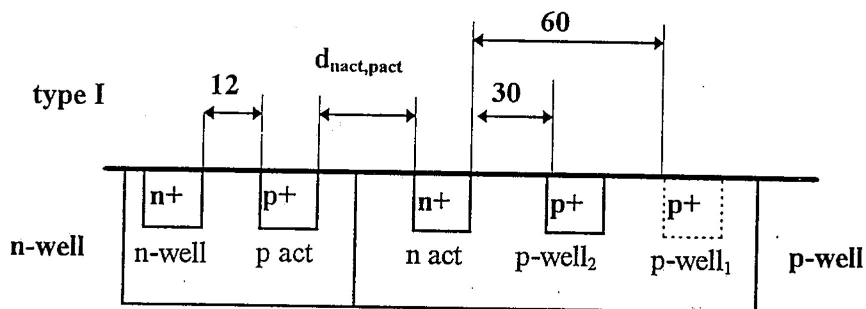


**Figure 6: Cross section of the RLUPB test structure (example for type Ix structure)**

## 2.3 Definitions

latch-up: a state in which a low-impedance path exists and persists from the $V_{dd}$ to the GND terminal following an injected current that triggers a parasitic four-layer bipolar structure. This refers to be the "on" state.

beta (β) npn: current gain of the parasitic npn transistor

beta (β) pnp: current gain of the parasitic pnp transistor

$I_t$, trigger current: in the "off" state the trigger current is defined as the minimum currrent to induce latch-up

$V_t$, trigger voltage: in the "off" state the trigger voltage is defined as the minimum voltage to induce latch-up

$I_h$, holding current: in the "on" state, the lowest current which will still allow the pnpn to remain in the conducting state

$V_h$, holding voltage: in the "on" state, the lowest voltage which will still allow the pnpn to remain in the conducting state.

Trigger and holding currents and voltages are in general determined according to figure 7.

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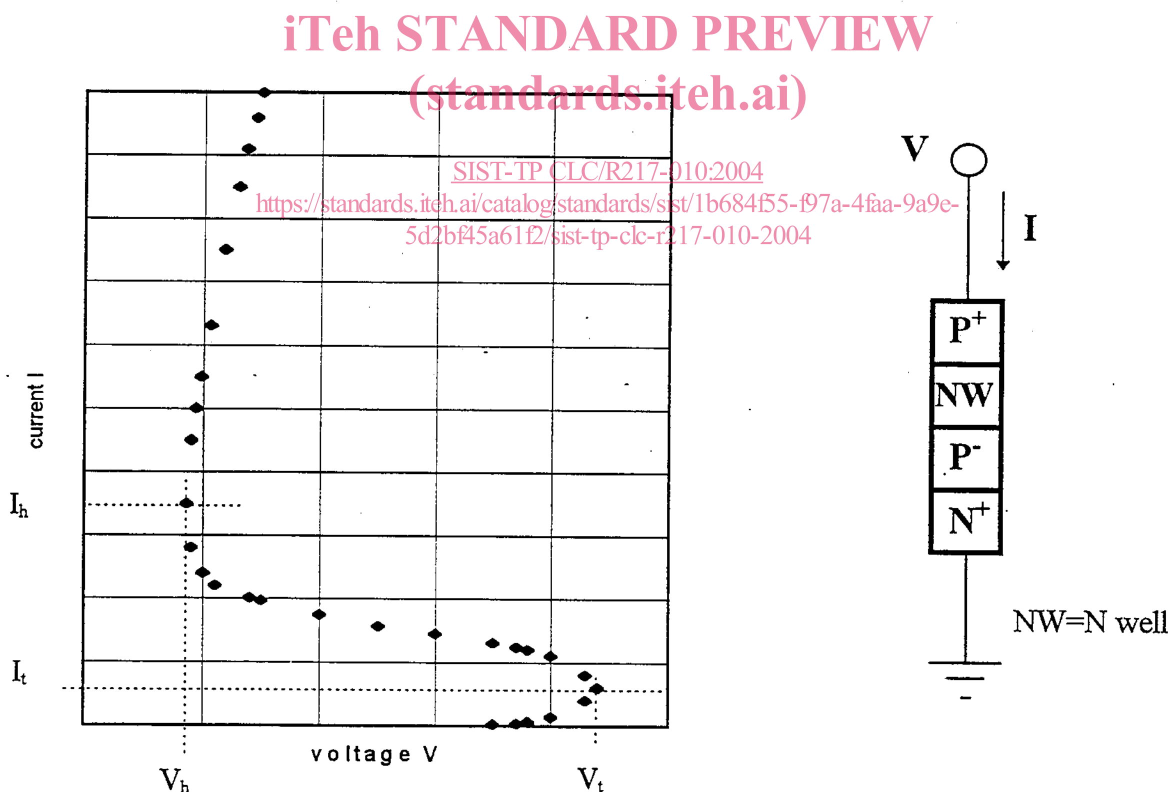


**Figure 7: Illustrative PNPN current/ voltage characteristics**

## 2.4 Test method

A cross section of both structure types I and II, including all parasitics is shown in figures 8 and 9. X corresponds to the minimum layout rule given by a certain technology (3.6 µm and 2.2 µm in the example, respectively).

Four types of measurements are proposed:

(1) Determination of the parasitic bipolar transistor parameters,

(2) Measurements of trigger and holding currents and voltages of the 4 layer structure due to $V_{dd}$ overstress,

(3) Measurement of the npn and pnp emitter injection currents necessary for latch-up triggering,

(4) Characterization of the sensitivity of the technology towards the injection of lateral substrate currents, not generated by the pnpn structure itself.

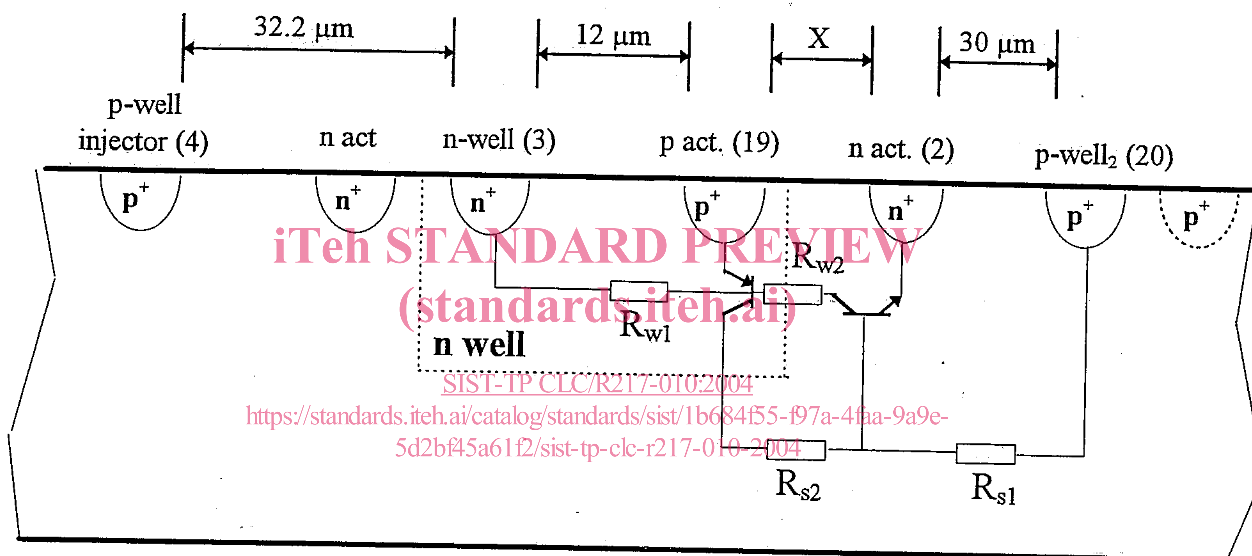


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**Figure 8: RLUPB structure, type I, e.g. X = 3.6µm (Ia), in brackets: bondpad number [7]**

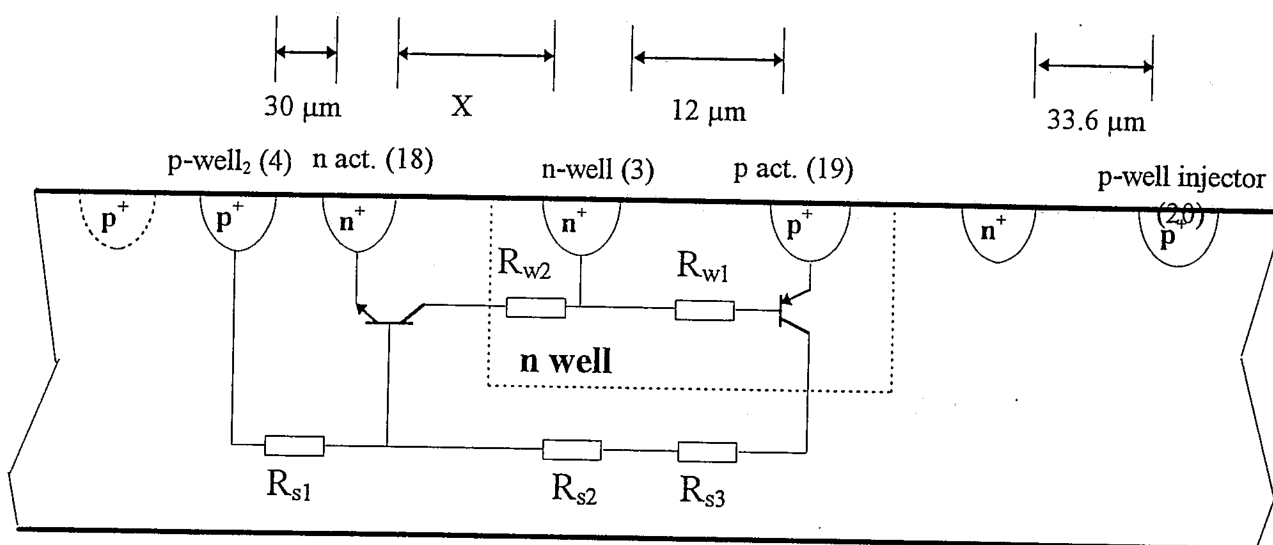


**Figure 9: RLUPB structure, type II, e.g. X = 2.2µm (IIa), in brackets: bondpad number [7]**

Each of these measurements will be explained below:

1. **Characterization of the parasitic bipolar transistors.** This consists of the determination of beta (β), and of the collector and emitter resistances of the parasitic npn and pnp bipolar transistors. This can be performed according to commonly used methods to characterize bipolar transistors (e.g. [13]).

**Table 1: Bipolar structures of RLUPB**

| **type** | **terminal** function | **structure Ia** type/ bondpad number | | **structure IIa** type/ bondpad number | |
|---|---|---|---|---|---|
| **npn transistor** | emitter | n act | 2 | n act | 18 |
| | base | p-well$_2$ | 20 | p-well$_2$ | 4 |
| | collector | n-well/ strap | 3 | n-well/ strap | 3 |
| **pnp transistor** | emitter | p act | 19 | p act | 19 |
| | base | n-well/ strap | 3 | n-well/ strap | 3 |
| | collector | p-well$_2$ | 20 | p-well$_2$ | 4 |

2. **Characterization of the latch-up sensitivity of the thyristor structure** due to $V_{dd}$ overstress:
this is determined by raising the voltage between n-well and p-well or substrate according to figure 7. This leads to well leakage and finally breakdown, resulting in turning on the parasitic npn, which will then further turn on the pnp.

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for structure Ia: $V_{ss}$ at bondpads 20, 2 (figure 8, bondpad numbers in brackets) apply voltage, while measuring current at bondpads 19 and 3 tied together,
for structure IIa: $V_{ss}$ at bondpads 18, 4 (figure 9, bondpad numbers in brackets) apply voltage, while measuring current at bondpads 19 and 3 tied together.
The output of this measurement is the determination of the trigger and holding currents and voltages according to $V_{dd}$ overstress of this test structure.

3. **Characterization of the npn and pnp emitter injection currents** necessary to trigger the other parasitic bipolar (fig.10):
for structure Ia:
   * pnp emitter current $I_{ep}$: force $I_{ep}$ (positive) at bondpad 19, while keeping the n-well (3) at 3.3V, and the p-well (20) and the npn emitter (2) at 0 V. Both emitter currents should be monitored as well as the n-well current. Latch-up occurs when the p-emitter current exceeds a certain threshold, leading to a sharp increase of both emitter currents (fig 10). This trigger point is the $I_{ep}$ to be measured.
   * npn emitter current $I_{en}$: force $I_{en}$ (negative) at bondpad 2, while keeping the p-well (20) at 0 V, and the n-well (3) and the p emitter of the pnp (19) at$V_{dd}$. The p-well current, as well as the current in the p-emitter (pad 19) should be monitored. At the trigger point of latch-up both emitter currents will increase rapidly. This is the $I_{en}$ to be measured.