SLOVENSKI STANDARD **SIST-TP CLC/R217-017:2004**

september 2004

Evalvacijske tehnike za preskušanje struktur zanesljivosti evropskega mini preskusnega čipa

Evaluation techniques of the reliability test structures of the European mini test chip

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ICS 35.240.10

Referenčna številka
SIST-TP CLC/R217-017:2004(en)

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CENELEC **R217-017**

REPORT February 1997

English version

Evaluation techniques of the reliability test structures of the European mini test chip

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved by CENELEC on 1996-07-02 and endorsed by the CENELEC Technical Board on 1996-12-09.

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Ref. No. R217-017:1997 E

Foreword

This CENELEC Report was prepared by the Technical Committee CENELEC TC 217, Electronic Design Automation (EDA). It was approved for publication by TC 217 on 1996-07-02 and endorsed by the CENELEC Technical Board on 1996-12-09.

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1 Introduction

This document is part of a series of documents describing a technology assessment system cycle of submicron CMOS technologies. The series consists of eight closely related documents [1, 2, 3, 4, 5, 6, 7, 8] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle[1] is the content of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS technologies down to 0.5 µm is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in [3]. The documentation of the measurements of these test structures is the objective of [4]. Document [5] contains the techniques used for the extraction of transistor model parameters. The purpose of document [6] is the presentation of a data exchange format which can be used with existing data evaluation programs. Test structures for a fast reliability assessment with respect to the major failure mechanisms in CMOS technologies are described in [7]. The measurement techniques required for the characterization of the reliability test structures are documented in [8]. The evaluation of results is subject of this document.

This paper together with [7] and [8] are dedicated to the reliability assessment of a submicron technology. The evaluation techniques described here can be applied to any relevant results gained in proper conducted reliability experiments.

The described evaluation techniques are applicable for CMOS technologies specifically for test structures described in [7] measured with methods described in [8]. The minimum feature sizes of the CMOS technologies range from 0.8 µm down to 0.5 µm.

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The validity of the test structures as well as the measurement and evaluation techniques has to be proven for the next generation of technologies (0.35 µm and less) and eventually adapted . The basic test structures mainly serve as test vehicles to obtain early results on failure mechanisms even in non-mature semiconductor technologies. In-depth reliability evaluation, e.g. for qualification purposes, may require additional structures and measurement techniques.

Evaluation techniques for the dominant failure mechanisms in submicrometer technologies
- **Latch up**
- **Hot Carrier**
- **Oxide Integrity**
- **Electromigration**

are described in detail.

The evaluations described are based on commonly used methods and are based on relatively simple models with their limitations. The failure criteria given in the text are chosen arbitrarily, however they are commonly used and accepted values. They serve as numbers which allow to compare technologies rather than estimate product reliability levels. Product reliability depends besides the inherent technology reliability also very much on a certain design which has to be taken into account to estimate product reliability.

[1] The Technology Assessment Support Center (TASC) provides detailed information about the computer programs which support the measurements and extraction routines. Send a fax or email to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart. Fax: +49-711-685-5930. Email: tasc@svlsi.mikro.uni-stuttgart.de

[2] This work is part of the JESSI Project AC 41 "Technology Assessment" and is sponsored by the national Public Authorities of Belgium, France and Germany

2 Latch-Up

2.1 Introduction

The potential for latch-up exists in all bulk CMOS integrated circuits because of the existence of parasitic pnpn paths in these structures. There is some improvement concerning latch-up hardness possible in using epitaxial instead of bulk material. In CMOS inverter structures, for example, the pnpn path runs from the p^+ source of the pMOS transistor, through the n-well, into the p-well or substrate and ends at the n^+ source of the nMOS. In its simplest form the equivalent circuit consists of a pnp transistor coupled with a npn transistor such that the pnp collector sources the base current of the npn transistor while the npn collector sinks the base current of the pnp transistor.

In [7] specific structures and methods are given for having a quick evaluation of the parasitic bipolar transistors which are, in CMOS integrated circuits, responsible for latch-up. Also the measurement techniques for determining the sensitivity of the technology with respect to latch-up on wafer level were described [8].

Since latch-up is also very dependent upon the layout, this method does not provide a means to determine the latch-up behaviour of real circuits. This is done by the existing JEDEC specification [9] describing latch-up in CMOS integrated circuits.

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2.2 Evaluation

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The results, as obtained from the measurements described in [8], can be used directly as they are to compare basic latch-up characteristics of CMOS technologies. No extrapolation techniques are necessary.

In module RLUPB [8], two types of latch-up structures are available. The different structures are dedicated to prove:
- the layout rules for the spacing of different active areas (type I),
- the rules for the placement of contacts i.e. spacing between similar types of active areas (type II).

The mentioned types again differ in the actual test structure layout (a, b and c respectively), they are designed based on :
- minimum allowed design rules (a),
- relaxed design rules (b),
- 90 % of the minimum distance of technologies between n^+ and p^+ active areas (c).

For latch-up comparisons, types Ia and IIa should be used. Normally only the layout rules have to be checked, therefore only structures drawn according the nominal layout rules have to be measured. This can be done using the structures Ia and IIa. The other structures can be used in the case latch-up occurs and to find out whether relaxed rules are sufficient to suppress latch-up and to get an idea how big the margin for latch-up is.

3 Hot Carrier Degradation of MOSFETs

3.1 Introduction

Hot carrier induced degradation of MOSFET parameters versus time is an important reliability concern in modern microcircuits. High energy carriers, also called hot carriers, are generated in MOSFET inversion layers by the large channel electric fields near the drain region of the MOSFET. The electric fields accelerate the carriers to effective temperatures above the lattice temperature. These hot carriers transfer energy to the lattice through phonon emission, as well as break bonds at the Si/ SiO_2 interface and in the SiO_2 itself. They also are injected into the SiO_2 and can be trapped there. The trapping or bond breaking creates oxide charge or interface traps that affect the channel carrier's mobility and the effective channel potential [10].

Hot carrier effects degrade MOSFET threshold voltage, transconductance, and drive current in all operating regimes. MOSFET design and IC process details can make certain parameters degrade faster than others. Both p- and n-channel MOSFETs are affected by hot carriers. N-channel devices are much more susceptible to damage than p-channel devices. Therefore emphasis is given to n-channel MOSFETs. Nevertheless also evaluation guidelines for p-channel MOSFETs are given.

Test structures to investigate hot carrier effects are described in [7] and the measurement methods are given in [8]. The following evaluation methods are used to extract characteristic values to compare and estimate the hot carrier behaviour of different technologies. To estimate the lifetime of a product with all the complications involved is not the goal of this technical report.

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3.2 Evaluation

The evaluation is based on the parameter shifts measured during DC stress tests using single MOSFET devices [8].

3.2.1 Data Analysis

All relative (e.g. $\Delta g_{m,max}$) parameter shifts are calculated regarding [10]:

$$Y(t) = |P(t)-P(init)| / |P(init)| \qquad (1)$$

where
Y(t) is the relative shift of any parameter value (P),
P(t) is the value of the parameter P at the time t, t is the accumulated stress time,
P(init) is the value of the parameter p at time zero (before applying stress)
with parameter P being e.g. $g_{m,max}$, $I_{ds,sat}$.
In the case of the threshold voltage shift (ΔV_{th}) often a absolute shift is used instead of a relative shift. The absolute shift is defined as:

$$Y(t) = P(t) - P(init). \qquad (2)$$

In this case Y(t) is an absolute shift of a parameter P(t).

In general these formulas can also be applied to determine an AC degradation (e.g. a frequency degradation of a ring oscillator).

3.2.2 Modelling of the Degraded Parameters

The change in each parameter shall be fitted to the following equation using a least-squares fit on:

$$\log Y(t) = n_1 * \log(t) + C1 \qquad (3)$$

An example is given in figure 1, where Y is the change in the parameter ΔV_{th}, and t is the cumulative stress time. The given dependence (3) exhibits a power law of the degradation in time. The factor n_i is a technology specific value. The lifetime T_{life} for each parameter should be interpolated or extrapolated from the data based on the C_i and n values from this least-squares fit. Often a saturation effect can be seen leading to different slopes. In this case it is recommended to use the slope seen at longer stress times to determine the lifetime for a certain parameter shift. T_{life} has to be determined by the choice of a certain shift (e.g. 10%) and a certain parameter (e.g. $g_{m,max}$).
In some cases the data fit a logarithmic law according to:

$$Y(t) = n_2 * \log(t) + C2 \qquad (4)$$

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An example is shown in figure 2. Particular attention has to be taken for p-channel transistors because the linearity of the degradation in a log-log scale concerning the threshold voltage and the saturation current is not always verified and extrapolation to the failure criteria can result in an underestimation of lifetime (worst case extrapolation). Many readouts are necessary to ensure the linearity.

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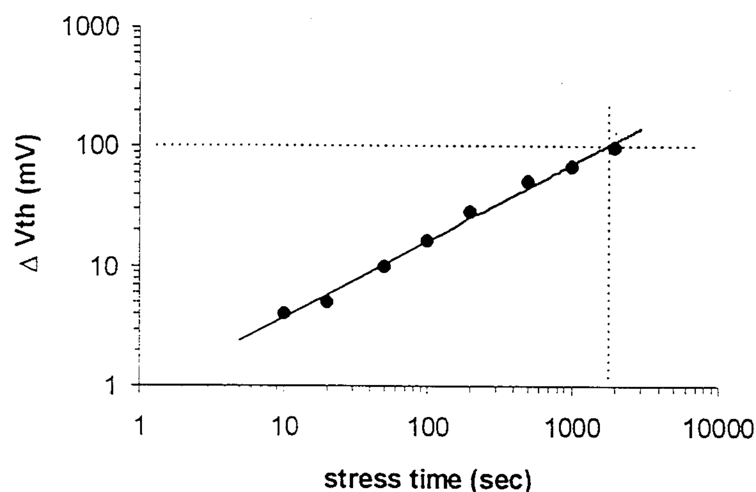

Figure 1: Example for the degradation following a power law, $T_{life} \approx 2000$ sec (100 mV V_{th} shift)

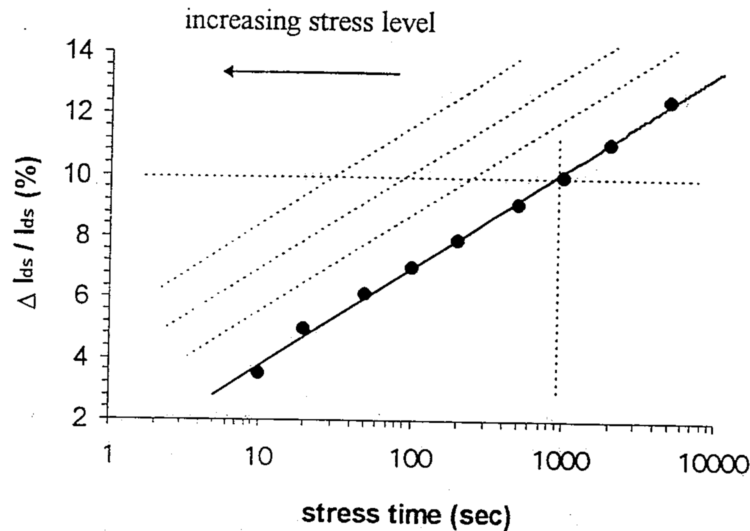

Figure 2: Example for a logarithmic degradation over time, $T_{life} \approx 1000$ sec (10 % I_{ds} shift)

Measurements have to be performed applying different stress levels. They should exhibit parallel curves (see fig.2) for these stress levels. From these plots T_{life} as a function of the stress can be determined for a certain failure criteria (e.g. $g_{m,max}$).

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3.2.3 Model for the Extrapolation to Nominal Conditions

Three models have been found to be available for the extrapolation of the results to nominal conditions. T_{life} represents the DC lifetime of a MOS device in each of the equations.
After C.Hu et al. [11] and J.J. Tzou et al. [12] the lifetime of n- and p-channel transistors can be modelled by the equations (5). This model is recommended to use and an example is given in figure 3.

n-channel: $T_{life} * I_{ds} = CN * (I_{sub}/I_{ds})^{-m}$ (5a)

p-channel: $T_{life} * I_{sub} = CP * (I_{sub}/I_{ds})^{-n}$ (5b)

with $m = \Phi_{it}/\Phi_{ie}$, $n = (\Phi_{it}*\lambda_h)/(\Phi_{ih}*\lambda_e)$

Φ_{it}: the critical electron energy for generating interface traps

Φ_{ie}, Φ_{ih}: electron and hole threshold energy for electron-hole pair generation, respectively

CN, CP: constants dependent of the technology under consideration

$\lambda_{e,h}$ are the mean free path length of electrons and holes, respectively.

Figure 3 shows an example based on equation (5a). The fraction I_{sub}/I_{ds} determines the stress levels used in different tests and corresponds to a certain stress condition $V_{ds,stress}$ and $V_{gs,stress}$. T_{life} are the corresponding values determined as described above. The technology dependent values for CN, CP and m, n can be extracted.

Based on figure 3 the lifetime for different operating conditions can be extracted by using the proper value for I_{sub} / I_{ds} and calculate τ based on log (τ*I_{ds}/W) and the value given by the extrapolated curve.

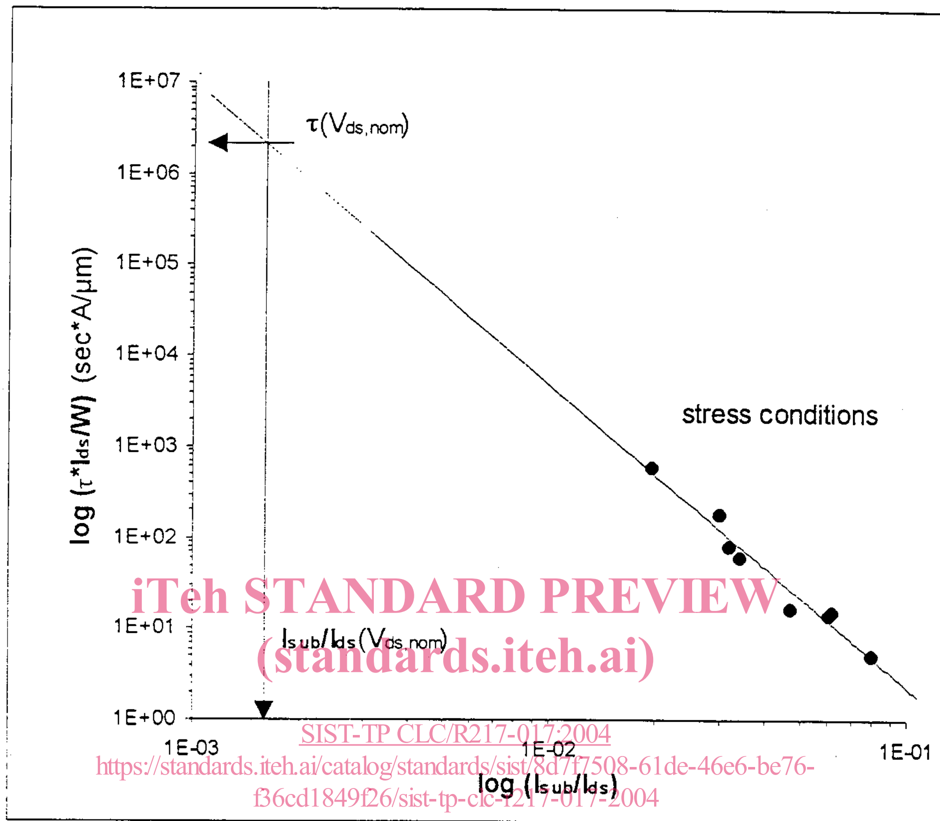

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Figure 3: Lifetime extraction for normal operating conditions

It is required to report lifetime values for transistors in the following operating conditions:
- nominal and maximum rating conditions ($V_{ds,nom}$ and $V_{ds,max}$),
- minimum and typical effective channel length ($L_{eff,min}$ and $L_{eff,typ}$) of the shortest transistors allowed by design rules.

These data have to be given for the described parameter shifts in [8].

The dependence of lifetime as a function of channel length is also very helpful for designers and it is recommended also to provide these data.

Besides lifetime results a complete report should comprise
- applied stress conditions,
- monitored parameter shift,
- lifetimes for different parameter shifts if available, containing also reverse measurements,
- channel geometries,
- extrapolation methods,
- statistics.