

**SLOVENSKI STANDARD**  
**SIST EN 60191-4:2014/A1:2018**  
**01-julij-2018**

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**Standardizacija mehanskih lastnosti polprevodniških elementov - 4. del: Kodirni sistem in klasifikacija oblik okrovov polprevodniških elementov - Dopolnilo A1 (IEC 60191-4:2013/A1:2018)**

Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages (IEC 60191-4:2013/A1:2018)

Mechanische Normung von Halbleiterbauelementen - Teil 4: Codierungssystem für Gehäuse und Eingruppierung der Gehäuse nach der Gehäuseform für Halbleiterbauelemente (IEC 60191-4:2013/A1:2018)

Normalisation mécanique des dispositifs à semi-conducteurs - Partie 4: Système de codification et classification en formes des structures des boîtiers pour dispositifs à semi-conducteurs (IEC 60191-4:2013/A1:2018)

**Ta slovenski standard je istoveten z: EN 60191-4:2014/A1:2018**

**ICS:**

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

**SIST EN 60191-4:2014/A1:2018**      **en**

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EUROPEAN STANDARD

EN 60191-4:2014/A1

NORME EUROPÉENNE

EUROPÄISCHE NORM

May 2018

ICS 31.080

English Version

Mechanical standardization of semiconductor devices - Part 4:  
Coding system and classification into forms of package outlines  
for semiconductor device packages  
(IEC 60191-4:2013/A1:2018)

Normalisation mécanique des dispositifs à semiconducteurs  
- Partie 4: Système de codification et classification en  
formes des structures des boîtiers pour dispositifs à  
semiconducteurs  
(IEC 60191-4:2013/A1:2018)

Mechanische Normung von Halbleiterbauelementen - Teil  
4: Codierungssystem für Gehäuse und Eingruppierung der  
Gehäuse nach der Gehäuseform für Halbleiterbauelemente  
(IEC 60191-4:2013/A1:2018)

This amendment A1 modifies the European Standard EN 60191-4:2014; it was approved by CENELEC on 2018-05-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this amendment the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This amendment exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

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European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

**EN 60191-4:2014/A1:2018 (E)****European foreword**

The text of document 47D/897/CDV, future edition 3 of IEC 60191-4:2013/A1, prepared by IEC/TC 47D "Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 60191-4:2014/A1:2018.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2019-02-01
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2021-05-01

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

**Endorsement notice**

The text of the International Standard IEC 60191-4:2013/A1:2018 was approved by CENELEC as a European Standard without any modification.

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IEC 60191-4

Edition 3.0 2018-03

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE

AMENDMENT 1  
AMENDEMENT 1

**Mechanical standardization of semiconductor devices –  
Part 4: Coding system and classification into forms of package outlines for  
semiconductor device packages**

**Normalisation mécanique des dispositifs à semiconducteurs –  
Partie 4: Système de codification et classification en formes des structures des  
boîtiers pour dispositifs à semiconducteurs**

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## FOREWORD

This amendment has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices.

The text of this amendment is based on the following documents:

CDV	Report on voting
47D/897/CDV	47D/904/RVC

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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Add, after Annexes A and B, the following new Annex C:

### **Annex C** (informative)

#### **Terminology of semiconductor package outlines**

To prevent misuse, misunderstanding and confusion of terminology of semiconductor package outline, correct terms and descriptions are required to be indicated in the international standards.

Correct terms and descriptions of semiconductor package outline including package code variations are listed in Table C.1.

**Table C.1 – Package name and parts name**

Classification	Term	Description
Package name	Ball Grid Array Package (BGA)	A package with the balls or bumps placed in a row of 3 x 3 or more, or in grid, on the upper or lower side of its body
Package name	Low Profile Ball Grid Array Package (LBGA)	BGA with the seated height of over 1,2 mm and up to 1,7 mm
Package name	Thin Ball Grid Array Package (TBGA)	BGA with the seated height of over 1,0 mm and up to 1,2 mm
Package name	Very Thin Ball Grid Array Package (VBGA)	BGA with the seated height of over 0,8 mm and up to 1,0 mm
Package name	Very-very Thin Ball Grid Array Package (WBGA)	BGA with the seated height of over 0,65 mm and up to 0,8 mm
Package name	Ultra-thin Ball Grid Array Package (UBGA)	BGA with the seated height of over 0,5 mm and up to 0,65 mm
Package name	Extra Thin Ball Grid Array Package (XBGA)	BGA with the seated height of up to 0,5 mm
Package name	Heat Sink Ball Grid Array Package (HBGA)	BGA with a heat sink
Package name	Heat Sink Low Profile Ball Grid Array Package (HLBGA)	LBGA with a heat sink
Package name	Heat Sink Thin Ball Grid Array Package (HTBGA)	TBGA with a heat sink
Package name	Heat Sink Very Thin Ball Grid Array Package (HVBGA)	VBGA with a heat sink
Package name	Heat Sink Very-very Thin Ball Grid Array Package (HWBGA)	WBGA with a heat sink
Package name	Heat Sink Ultra-thin Ball Grid Array Package (HUBGA)	UBGA with a heat sink
Package name	Heat Sink Extra Thin Ball Grid Array Package (HXBGA)	XBGA with a heat sink
Package name	Fine Pitch Ball Grid Array Package (FBGA)	BGA with the terminal pitch of up to 0,8 mm
Package name	Low Profile Fine Pitch Ball Grid Array Package (LFBGA)	FBGA with the seated height of over 1,2 mm and up to 1,7 mm
Package name	Thin Fine Pitch Ball Grid Array Package (TFBGA)	FBGA with the seated height of over 1,0 mm and up to 1,2 mm
Package name	Very Thin Fine Pitch Ball Grid Array Package (VFBGA)	FBGA with the seated height of over 0,8 mm and up to 1,0 mm
Package name	Very-very Thin Fine Pitch Ball Grid Array Package (WFBGA)	FBGA with the seated height of over 0,65 mm and up to 0,8 mm

Classification	Term	Description
Package name	Ultra-thin Fine Pitch Ball Grid Array Package (UFPGA)	FBGA with the seated height of over 0,5 mm and up to 0,65 mm
Package name	Extra Thin Fine Pitch Ball Grid Array Package (XFPGA)	FBGA with the seated height of up to 0,5 mm
Package name	Terminal for stack Fine Pitch Ball Grid Array Package (PFPGA)	FBGA with the terminals for layer stack
Package name	Terminal for stack Low Profile Fine Pitch Ball Grid Array Package (PLFPGA)	LFBGA with the terminals for layer stack
Package name	Terminal for stack Thin Fine Pitch Ball Grid Array Package (PTFPGA)	TFBGA with the terminals for layer stack
Package name	Terminal for stack Very Thin Fine Pitch Ball Grid Array Package (PVFPGA)	VFBGA with the terminals for layer stack
Package name	Terminal for stack Very-very Thin Fine Pitch Ball Grid Array Package (PVFPGA)	WFBGA with the terminals for layer stack
Package name	Terminal for stack Ultra-thin Fine Pitch Ball Grid Array Package (PUFPGA)	UFPGA with the terminals for layer stack
Package name	Terminal for stack Extra Thin Fine Pitch Ball Grid Array Package (XFPGA)	XFPGA with the terminals for layer stack
Package name	Interstitial Ball Grid Array Package (IBGA)	Interstitial BGA
Package name	Plastic Ball Grid Array Package (P-BGA)	Plastic BGA
Package name	Ceramic Ball Grid Array Package (C-BGA)	Ceramic BGA
Package name	Silicon Fine Pitch Ball Grid Array Package (S-FBGA)	Silicon FBGA
Package name	Dual Inline Package (DIP)	A package with the leads extended from the two sides of its body and used for through-hole mounting
Package name	Shrink Dual Inline Package (SDIP)	Shrink DIP
Package name	Heat Sink Dual Inline Package (HDIP)	DIP with a heat sink
Package name	Heat Sink Shrink Dual Inline Package (HSDIP)	SDIP with a heat sink
Package name	Piggyback Dual Inline Package (PDIP)	Piggyback DIP
Package name	Plastic Dual Inline Package (P-DIP)	Plastic DIP



Classification	Term	Description
Package name	Ceramic Dual Inline Package (C-DIP)	Ceramic DIP
Package name	Glass-Sealed Ceramic Dual Inline Package (G-DIP)	Glass-sealed ceramic DIP
Package name	Glass-Sealed Ceramic Window Dual Inline Package (G-DDIP)	Glass-sealed ceramic DIP with a window
Package name	Dual Tape Carrier Package (DTP)	A package with the leads extended from the two sides of its body and consisting of the tapes
Package name	Dual Tape Carrier Package Type 1 (DTP(1))	DTP Type-1
Package name	Dual Tape Carrier Package Type 2 (DTP(2))	DTP Type-2
Package name	Land Grid Array Package (LGA)	A package without pins and with the lands placed in a row of 3 x 3 or more, or in grid, on the upper or lower side of its body
Package name	Low Profile Land Grid Array Package (LLGA)	LGA with the seated height of over 1,2 mm and up to 1,7 mm
Package name	Thin Land Grid Array Package (TLGA)	LGA with the seated height of over 1,0 mm and up to 1,2 mm
Package name	Very Thin Land Grid Array Package (VLGA)	LGA with the seated height of over 0,8 mm and up to 1,0 mm
Package name	Very-very Thin Land Grid Array Package (WLGA)	LGA with the seated height of over 0,65 mm and up to 0,8 mm
Package name	Ultra-thin Land Grid Array Package (ULGA)	LGA with the seated height of over 0,5 mm and up to 0,65 mm
Package name	Extra Thin Land Grid Array Package (XLGA)	LGA with the seated height of up to 0,5 mm
Package name	Heat Sink Land Grid Array Package (HLGA)	LGA with a heat sink
Package name	Heat Sink Low Profile Land Grid Array Package (HLLGA)	LLGA with a heat sink
Package name	Heat Sink Thin Land Grid Array Package (HTLGA)	TLGA with a heat sink
Package name	Heat Sink Very Thin Land Grid Array Package (HVLGA)	VLGA with a heat sink
Package name	Heat Sink Very-very Thin Land Grid Array Package (HWLGA)	WLGA with a heat sink
Package name	Heat Sink Ultra-thin Land Grid Array Package (HULGA)	ULGA with a heat sink
Package name	Heat Sink Extra Thin Land Grid Array Package (HXLGA)	XLGA with a heat sink