SLOVENSKI STANDARD
SIST EN IEC 60191-1:2018

01-junij-2018

Nadomešča:
SIST EN 60191-1:2008

Standardizacija mehanskih lastnosti polprevodniških elementov - 1. del: Splošna pravila za pripravo tehničnih risb diskretnih elementov (IEC 60191-1:2018)

Mechanical standardization of semiconductor devices - Part 1: General rules for the preparation of outline drawings of discrete devices (IEC 60191-1:2018)

Mechanische Normung von Halbleiterbauelementen - Teil 1: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von Einzelhalbleiterbauelementen (IEC 60191-1:2018)

Normalisation mécanique des dispositifs à semi-conducteurs - Partie 1: Règles générales pour la préparation des dessins d'encombrement des dispositifs discrets (IEC 60191-1:2018)

Ta slovenski standard je istoveten z: **EN IEC 60191-1:2018**

ICS:

01.100.25	Risbe s področja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

SIST EN IEC 60191-1:2018 **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN IEC 60191-1

March 2018

ICS 31.080.01

Supersedes EN 60191-1:2007

English Version

Mechanical standardization of semiconductor devices - Part 1: General rules for the preparation of outline drawings of discrete devices (IEC 60191-1:2018)

Normalisation mécanique des dispositifs à semi-conducteurs - Partie 1: Règles générales pour la préparation des dessins d'encombrement des dispositifs discrets (IEC 60191-1:2018)

Mechanische Normung von Halbleiterbauelementen - Teil 1: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von Einzelhalbleiterbauelementen (IEC 60191-1:2018)

This European Standard was approved by CENELEC on 2018-02-27. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

European foreword

The text of document 47D/886/CDV, future edition 3 of IEC 60191-1, prepared by IEC/SC 47D "Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 60191-1:2018.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2018-11-27
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2021-02-27

This document supersedes EN 60191-1:2007.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 60191-1:2018 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60191-6 (series)	NOTE	Harmonized as EN 60191-6 (series).
ISO 5459:2011	NOTE	Harmonized as EN ISO 5459:2011 (not modified).

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 60191-2	-	Mechanical standardization of semiconductor devices - Part 2: Dimensions	-	-
IEC 60191-4	-	Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4	-
IEC 60191-6-1	-	Mechanical standardization of semiconductor devices - Part 6-1: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for gull-wing lead terminals	EN 60191-6-1	-
IEC 60191-6-3	-	Mechanical standardization of semiconductor devices - Part 6-3: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Measuring methods for package dimensions of quad flat packs (QFP)	EN 60191-6-3	-
IEC 60191-6-20	-	Mechanical standardization of semiconductor devices - Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Measuring methods for package dimensions of small outline J-lead packages (SOJ)	EN 60191-6-20	-
IEC 60191-6-21	-	Mechanical standardization of semiconductor devices - Part 6-21: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Measuring methods for package dimensions of small outline packages (SOP)	EN 60191-6-21	-

IEC 60191-1

Edition 3.0 2018-01

INTERNATIONAL STANDARD

Mechanical standardization of semiconductor devices –
Part 1: General rules for the preparation of outline drawings of discrete devices

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

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CONTENTS

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 1: General rules for the preparation of outline drawings of discrete devices

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

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International Standard IEC 60191-1 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices.

This third edition cancels and replaces the second edition published in 2007. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the Scope has been extended to include surface-mounted semiconductor devices with a lead count less than 8;
b) a definition of the term "stand-off" has been added;
c) the methods for locating the datum have been extended to be suitable for SMD-packages;
d) the visual identification of terminal position one for automatic handling has been clarified;
e) the rules for the drawing of terminals have been clarified;

f) Table A.1 has been completed with symbols specifically for SMD-packages;

g) Annex B "Standardization philosophy" has been deleted;

h) a normative Annex with special rules for SMD-packages has been added;

i) the examples of semiconductor device drawings have been aligned to state-of-the-art packages including SMD-packages.

The text of this standard is based on the following documents:

CDV	Report on voting
47D/886/CDV	47D/896/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60191 series, published under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 1: General rules for the preparation of outline drawings of discrete devices

1 Scope

This part of IEC 60191 gives guidelines on the preparation of outline drawings of discrete devices, including discrete surface-mounted semiconductor devices with lead count less than 8.

For the preparation of outline drawings of surface-mounted discrete devices with a lead count higher or equal to 8, IEC 60191-6 should be referred to as well.

The primary object of these drawings is to indicate the space to be allowed for devices in equipment, together with other dimensional characteristics required to ensure mechanical interchangeability.

Complete interchangeability involves other considerations such as the electrical and thermal characteristics of the semiconductor devices concerned.

The international standardization represented by these drawings therefore encourages the manufacturers of devices to comply with the tolerances shown on the drawings in order to extend their range of customers internationally. It also gives equipment designers an assurance of mechanical interchangeability between the devices obtained from suppliers in different countries, provided they allow the space in their equipment that is indicated by the drawings and take note of the more precise information on bases, studs, etc.

NOTE Additional details of reference letter symbols used in this document are given in Annex A.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-2, *Mechanical standardization of semiconductor devices – Part 2: Dimensions*

IEC 60191-4, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*

IEC 60191-6-1, *Mechanical standardization of semiconductor devices – Part 6-1: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for gull-wing lead terminals*

IEC 60191-6-3, *Mechanical standardization of semiconductor devices – Part 6-3: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Measuring methods for package dimensions of quad flat packs (QFP)*

IEC 60191-6-20, *Mechanical standardization of semiconductor devices – Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Measuring methods for package dimensions of small outline J-lead packages (SOJ)*

IEC 60191-6-21, *Mechanical standardization of semiconductor devices – Part 6-21: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Measuring methods for package dimensions of small outline packages (SOP)*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
device outline drawing
drawing that includes all dimensional characteristics required for the mechanical interchangeability of the complete device

Note 1 to entry: The device outline drawing includes the case or body, all terminals and the locating tab if present.

3.2
terminal
part of the semiconductor device primarily used in making an electrical, mechanical or thermal connection

EXAMPLE Flexible leads, rigid leads, pins, studs, etc.

3.3
case outline drawing
drawing that includes all dimensional characteristics required for the mechanical interchangeability of the case or body

Note 1 to entry: The case outline drawing does not include the dimensions of the terminals or the locating tab if present, but their positions are shown by dotted lines.

3.4
base drawing
drawing that includes all dimensional characteristics required for the mechanical interchangeability of the terminals and mechanical index

Note 1 to entry: Examples of these characteristics are: lead length, lead diameters with controlled zones, lead spacing, pitch circle diameter, thickness, width and length of a tab, etc.

Note 2 to entry: The diameter or major axis of the case outline should not be given on the base drawing.

Note 3 to entry: Many semiconductor devices have identical cases, but differ in the number or the length of terminals. It is also possible to have the same type of base associated with cases that are not identical.

Consequently, there are advantages in having:

a) a single drawing including only the dimensional characteristics of the case outline and separate drawings for the various bases which can be associated with this case outline,

   or

b) a single drawing including only the dimensional characteristics of the base and separate drawings for the various case outlines which can be associated with this base.

3.5
mechanical index
locating feature, or that portion of the device specifically designed to provide orientation

Note 1 to entry: Examples of a mechanical index are: key, keyway, locating tab, etc.