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Semiconductor devices - Mechanical and climatic test methods - Part 41: Standard reliability testing methods of non-volatile memory devices (IEC 60749-41:2020)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 41: Standardisierte Prüfverfahren für die Zuverlässigkeit von nichtflüchtigen Speicher-Bauelementen (IEC 60749-41:2020)

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European foreword

The text of document 47/2631/FDIS, future edition 1 of IEC 60749-41, prepared by IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 60749-41:2020.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2021-05-26
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Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 60749-6	-	Semiconductor devices - Mechanical and climatic test methods - Part 6: Storage at high temperature	EN 60749-6	-
IEC 60749-23	-	Semiconductor devices - Mechanical and climatic test methods - Part 23: High temperature operating life	EN 60749-23	-
JESD47	-	Stress-Test-Driven Qualification of Integrated Circuits	-	-
JESD94	-	Application Specific Qualification Using Knowledge Based Test Methodology	-	-

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MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2631/FDIS	47/2643/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

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A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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INTRODUCTION

The stress tests described in this part of IEC 60749 are intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention).

The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. The data retention stress can be used as a proxy to replace the high temperature storage life test when the temperature and time meet or exceed qualification requirements. Cross-temperature testing for writing and reading across the data sheet temperature range can be considered when there are demonstrated sensitivities for programming at low and reading at high temperatures or vice versa. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) can be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

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