SLOVENSKI STANDARD
SIST EN 62751-2:2014/oprA1:2018

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Ugotavljanje izgub moči v napetostnih pretvorniških ventilih za visokonapetostne enosmerne sisteme - 2. del: Modularni večnivojski pretvorniki

Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems - Part 2: Modular multilevel converters

Bestimmung der Leistungsverluste in Spannungszwischenkreis-Stromrichtern (VSC) für Hochspannungsgleichstrom(HGÜ)-Systeme - Teil 2: Modulare Mehrpunkt-Stromrichter

Pertes de puissance dans les valves à convertisseur de source de tension (VSC) des systèmes en courant continu à haute tension (CCHT) - Partie 2: Convertisseurs multiniveaux modulaires

Ta slovenski standard je istoveten z: **EN 62751-2:2014/prA1:2018**

ICS:

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2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

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22F/479/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

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IEC SC 22F : POWER ELECTRONICS FOR ELECTRICAL TRANSMISSION AND DISTRIBUTION SYSTEMS

SECRETARIAT: Russian Federation	SECRETARY: Mr Lev Travin
OF INTEREST TO THE FOLLOWING COMMITTEES: TC 115	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.

FUNCTIONS CONCERNED:

☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY

☒ SUBMITTED FOR CENELEC PARALLEL VOTING **Attention IEC-CENELEC parallel voting** The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting. The CENELEC members are invited to vote through the CENELEC online voting system.	☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING

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TITLE:

Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems - Part 2: Modular multilevel converters

PROPOSED STABILITY DATE: 2025

NOTE FROM TC/SC OFFICERS:

This document is circulated as a CDV in accordance with the decision taken at SC 22F meeting held in Xi'an, China, on October 23-24, 2017 (see 22F/472/RM, Item 9, Decision 2017-07, Action 2017-04). The Working Draft of the Amendment was developed by SC 22F Maintenance Team 31 (convenor Mr. Colin Davidson, Great Britain).

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FOREWORD

This amendment has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment.

The text of this amendment is based on the following documents:

FDIS	Report on voting
22F/xxx/FDIS	22F/xxx/RVD

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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3 Terms, definitions, symbols and abbreviated terms

3.1.11
no-load operating state

Add note:

NOTE: In the no-load state, in principle no switching should occur as the valve is blocked. However in some designs it may be necessary to make occasional switching operations to balance voltages between different parts of the converter. Here some losses may occur and need to be accounted for.

4 General conditions

4.1 General

Replace the abbreviation "CTLC" by "CTL".

Replace "IEC TR 62543" by "IEC/TR 62543".

4.2 Principles for loss determination

Add to the end of the first paragraph:

The manufacturer shall justify, in the loss calculation report, how the uncertainties have been considered.

Replace the last two sentences of the third paragraph by:

In practice this measurement would require the use of state-of-the-art measurement equipment that rivals the best equipment available at national metrology institutes. To date, although some industry/academic partnership projects have demonstrated prototypes of measurement equipment claiming sufficient accuracy, there is little industry experience with using such equipment on site. The feasibility of using laboratory measurements on VSC valves to support a more accurate determination of valve losses is now under study in CIGRÉ WG B4-75.

4.4 Loss calculation method

Replace the first sentence of the second paragraph by:

An important requirement for such simulations is an accurate modelling of the system under investigation.

4.5.2 Input data for numerical simulations

Replace the last item of the bulleted list by:

- For calculating converter valve currents and MMC building block capacitor currents, which are the basis for the calculation of corresponding losses, it is sufficient to use a simplified model in which the on-state and switching characteristics of the IGBTs and diodes are represented by worst-case characteristics applicable to their maximum rated junction temperature.

- For the detailed calculation of losses, the simulation shall also consider the junction temperature dependent semiconductor properties, such as on-state voltages, switching and recovery losses. These properties are based on the characterisation testing as described in IEC 62751-1:2014, 4.4.2. The steady-state junction temperatures of the semiconductors are calculated iteratively for the relevant operating point to derive the semiconductor losses.

4.5.3 Input data coming from numerical simulations

Add, after the last sentence:

The mean and rms currents in IGBTs and diodes are not required if conduction losses in IGBTs and diodes are calculated using polynomials as discussed in 5.1.

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4.5.4 Converter station data

Change the sixth bullet point of the list to read:

number of VSC levels per cell (for CTL designs);

Add new sub-clause:

4.6 Contents and structure of valve loss determination report

The manufacturer or bidder shall prepare and submit to the purchaser a detailed report explaining how the losses in the VSC valves have been determined and including a breakdown of the valve losses into the constituent parts P_{V1} to P_{V9} for each operating condition at which losses are required to be guaranteed.

At the bid stage, and (where requested in the contract) after contract award but before the manufacturing of valve components, the report shall document the assumptions used in arriving at the calculated value of losses. After manufacturing, the report shall document the actual values of test data derived from characterisation tests and routine tests on components.

Although a breakdown of the valve losses into the constituent parts P_{V1} to P_{V9} is requested, only the total valve losses P_{VT} shall be subject to financial evaluation.

A recommended list of data to be included in the report is presented in Annex B,

5 Conduction losses

5.1 General

Add at the end of 5.1:

To simplify the process of mathematically analysing conduction losses, the on-state voltage of IGBTs and diodes is usually represented as a piecewise-linear approximation with a threshold voltage V_0 and a slope resistance R_0, as shown on Figure 2 of IEC 62751-1.

It is possible to obtain greater accuracy by using a more exact model of the device on-state voltage (for example, using a polynomial function to represent the on-state voltage) rather than the piecewise linear approximation, and then performing a direct numerical integration. However, the piecewise-linear approximation is preferred because it simplifies the calculation process, allows greater transparency and still permits good accuracy to be obtained, provided the measurements used to derive the piecewise-linear approximation are made at appropriate values of current. Therefore it is recommended that V_0 and R_0 are determined by measuring on-state voltage at 100 % and 33 % of the device rated current and performing a linear extrapolation.

In the event that the purchaser prefers to use the more accurate method using a polynomial function then this shall be clearly stated in the purchasing specification and all bidders are expected to calculate power losses in a comparable way.

5.2 IGBT conduction loss

Replace all text and equations (2) – (5) after explanations of values for equation (1) by:

By means of numerical simulation the currents shall be calculated for the IGBTs T1 and T2 for each MMC building block, respectively:

$$I_{\mathrm{T1av}} = \frac{1}{t_{\mathrm{i}}} \cdot \int_0^{t_{\mathrm{i}}} i_{\mathrm{T1}}(t) \cdot dt \tag{2}$$

$$I_{\mathrm{T2av}} = \frac{1}{t_{\mathrm{i}}} \cdot \int_0^{t_{\mathrm{i}}} i_{\mathrm{T2}}(t) \cdot dt \tag{3}$$

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$$I_{\mathrm{T1rms}} = \sqrt{\frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{T1}}(t)^{2} \cdot dt} \tag{4}$$

$$I_{\mathrm{T2rms}} = \sqrt{\frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{T2}}(t)^{2} \cdot dt} \tag{5}$$

where

t_{i} is the integration time used in the simulation;

t_{i} shall not be less than 1 s.

If different IGBT types are used for T1 and T2, corresponding values for threshold voltages and slope resistances shall be used accordingly.

5.3 Diode conduction losses

Replace all text and equations (7) – (10) after explanations of values for equation (6) by:

By means of numerical simulation the currents shall be calculated for the diodes D1 and D2 for each MMC building block, respectively:

$$I_{\mathrm{D1av}} = \frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{D1}}(t) \cdot dt \tag{7}$$

$$I_{\mathrm{D2av}} = \frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{D2}}(t) \cdot dt \tag{8}$$

$$I_{\mathrm{D1rms}} = \sqrt{\frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{D1}}(t)^{2} \cdot dt} \tag{9}$$

$$I_{\mathrm{D2rms}} = \sqrt{\frac{1}{t_{\mathrm{i}}} \cdot \int_{0}^{t_{\mathrm{i}}} i_{\mathrm{D2}}(t)^{2} \cdot dt} \tag{10}$$

where

t_{i} is the integration time used in the simulation;

t_{i} shall not be less than 1 s.

If different diode types are used for D1 and D2, corresponding values for threshold voltages and slope resistances shall be used accordingly.

5.4 Other conduction losses

Replace the second sentence of the first paragraph by:

For modular multi-level converters this mainly consists of interconnecting busbars. Losses in valve reactors shall be considered separately from valve losses and calculated using the principles defined for AC filter reactors in IEC 61803.

9 Other losses

9.1 Snubber circuit losses

Replace the note by the following, and include it in the main text:

Including a snubber parallel to a VSC valve level influences the turn-on/turn-off behaviour of the IGBT/diode which means that the snubber circuits shall be correctly represented during the characterisation tests on the semiconductor devices.

9.2.1 General

Replace the first sentence of the fourth paragraph by:

The power consumption of each valve electronics unit should be determined by direct measurement on a sample of real valve electronics units under representative switching conditions (voltage, current, switching frequency etc). Tests shall be performed on a minimum quantity of valve electronics units equivalent to five submodules or 10 VSC valve levels (for the CTL design).

Annex A: Description of power loss mechanisms in MMC valves

A.1 Introduction to MMC Converter topology

Figure A.2

Replace “VSC valve leve” by “VSC valve level”.

Figure A.3

Replace “I_L” by “I_C”.

A.2.1 Simplified analysis with voltage and current in phase

Figure A.4

Replace “$I_L G\sqrt{2/2}$” by “$I_C \times \sqrt{2}/2$ ”.

Replace “$I_d/3+I_L \times \sqrt{2/2} \approx I_{dc}$” by “$I_d/3+ I_C \times \sqrt{2}/2 \approx I_{dc}$ ”

A.2.3 Effects of third harmonic injection

Figure A.6

Replace “I_L” by “I_C”.

A.3.1 Description of conduction paths

Figure A.9

Replace the existing title of Figure 9

Typical patterns of conduction for inverter operation (left) and rectifier operation (right)

by a new title:

Typical patterns of conduction for inverter operation (left) and rectifier operation (right), based on the submodule configuration of Figure A.7 (a).

Figure A.10

Replace “I_L” by “I_C”.

Replace the first sentence in paragraph 5 from the end of subclause A.3.1:

All series connected MMC building blocks will be stressed with the same switching events, but at different occasions.

by the following sentence

Although different MMC building blocks in the valve experience switching events at different times, on average the stress is the same on all series-connected MMC building blocks in the valve.

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A.3.2.1 Approximate analytical solution

Replace the existing text of A.3.2.1 by the following text:

It will be noted from Figure A.8 that at any time there is always one, and only one, current path conducting in each MMC building block.

If the on-state voltage characteristics of the four switch positions in the MMC building block were identical, calculation of the semiconductor device conduction losses would be straightforward, since there would be no need to know the operating state of the MMC building block at any time. The total semiconductor conduction loss per MMC building block would then simply be given by:

$$P_{\mathrm{cond}} = N_c\left(V_0 \cdot I_{\mathrm{vav}} + R_0 \cdot I_{\mathrm{vrms}}{}^2\right) \qquad \text{(A.1)}$$

where

N_c is the number of series-connected semiconductor devices per switch position;

V_0, R_0 are the threshold voltage and slope resistance of the device;

I_{vav} is the mean value of the rectified current in the valve, averaged over one power-frequency cycle (Figure A.13).

$$I_{\mathrm{vav}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} \left| i_{\mathrm{vtt}}(\omega t) \right| \cdot d(\omega t) \qquad \text{(A.2)}$$

where

$i_{vtt}(\omega t)$ is the instantaneous current between the terminals of the valve

NOTE I_{vav} is not the same as the mean valve current, which is simply $I_d/3$. For these purposes, the rectified current is needed because current will only flow in those semiconductor device(s) which are forward biased.

I_{vrms} is the rms current in the valve, averaged over one power-frequency cycle

$$I_{\mathrm{vrms}} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} i_{\mathrm{vtt}}(\omega t)^2 \cdot d(\omega t)} \qquad \text{(A.3)}$$