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SLOVENSKI STANDARD
SIST EN IEC 62433-6:2021

01-januar-2021

Modeliranje integriranih vezij (IC) za elektromagnetno združljivost (EMC) - 6. del: Modeli integriranih vezij za simulacijo impulzno odpornega obnašanja - Modeliranje impulzne odpornosti (ICIM-CPI) (IEC 62433-6:2020)

EMC IC modelling - Part 6: Models of integrated circuits for pulse immunity behavioural simulation - Conducted pulse immunity modelling (ICIM-CPI) (IEC 62433-6:2020)

EMV-IC-Modellierung - Teil 6: Modelle integrierter Schaltungen für die Simulation des Verhaltens bei Störfestigkeit gegen Impulse - Modellierung der Störfestigkeit gegen leitungsgeführte Impulse (ICIM-CPI) (IEC 62433-6:2020)

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Modèles de circuits intégrés pour la CEM - Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions - Modélisation de l'immunité aux impulsions conduite (ICIM-CPI) (IEC 62433-6:2020)

Ta slovenski standard je istoveten z: EN IEC 62433-6:2020

ICS:

31.200	Integrirana vezja, mikroelektronika	Integrated circuits. Microelectronics
33.100.20	Imunost	Immunity

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EMC IC modelling - Part 6: Models of integrated circuits for Pulse immunity behavioural simulation - Conducted Pulse Immunity (ICIM-CPI) (IEC 62433-6:2020)

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European foreword

The text of document 47A/1090/CDV, future edition 1 of IEC 62433-6, prepared by SC 47A "Integrated circuits" of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62433-6:2020.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2021-07-27
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2023-10-27

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

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IEC 62433-2:2017	NOTE	Harmonized as EN 62433-2:2017 (not modified)
CISPR 16-1-4:2019	NOTE	Harmonized as EN IEC 55016-1-4:2019 (not modified)
CISPR 17	NOTE	Harmonized as EN 55017

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Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 61000-4-2	-	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test	EN 61000-4-2	-
IEC 61000-4-4	-	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	-
IEC 62215-3	-	Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method	EN 62215-3	-
IEC 62433-1	-	EMC IC modelling - Part 1: General modelling framework	EN IEC 62433-1	-
IEC 62433-4	-	EMC IC modelling - Part 4: Models of integrated circuits for RF immunity behavioural simulation - Conducted immunity modelling (ICIM-CI)	EN 62433-4	-
IEC 62615	-	Electrostatic discharge sensitivity testing - Transmission line pulse (TLP) - Component level	-	-

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Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

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Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions – Modélisation de l'immunité aux impulsions conduites (ICIM-CPI)

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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

FOREWORD

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International Standard IEC 62433-6 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

CDV	Report on voting
47A/1090/CDV	47A/1098/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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A list of all parts in the IEC 62433 series, published under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

1 Scope

The objective of this part of IEC 62433 is to describe the extraction flow for deriving an immunity macro-model of an Integrated Circuit (IC) against conducted Electrostatic Discharge (ESD) according to IEC 61000-4-2 and Electrical Fast Transients (EFT) according to IEC 61000-4-4.

The model addresses physical damages due to overvoltage, thermal damage and other failure modes. Functional failures can also be addressed.

This model allows the immunity simulation of the IC in an application. This model is commonly called "Integrated Circuit Immunity Model Conducted Pulse Immunity", ICIM-CPI.

The described approach is suitable for modelling analogue, digital and mixed-signal ICs. Several terminals of an IC can be part of a single model (e.g. input, output and supply pins). The implementation of the model is capable of representing the non-linear behaviour of overvoltage protection circuits.

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The model can be implemented for the use in different software tools for circuit simulation in time-domain. The described modelling approach allows simulating device failure due to ESD or EFT at component and system level considering all components necessary for the immunity simulation of an IC, such as a PCB or external protection elements.

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This document demonstrates, in detail, the construction of models in a defined XML-based format which is suitable for the exchange of models without any deeper knowledge of the semiconductor circuit. However, the model functionality can be implemented in different formats including, but not limited to, tables, SPICE[1] [1] netlists, hardware description languages such as VHDL-AMS [2] and Verilog-AMS [3].

This document provides:

- the description of ICIM-CPI macro-model elements representing electrical, thermal or logical behaviour of the IC.
- a universal data exchange format based on XML.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

[1] Numbers in square brackets refer to the bibliography.

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IEC 61000-4-4, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 62215-3, *Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method*

IEC 62433-1, *EMC IC modelling – Part 1: General modelling framework*

IEC 62433-4:2016, *EMC IC modelling – Part 4: Models of integrated circuits for RF immunity behavioural simulation – Conducted immunity modelling (ICIM-CI)*

IEC 62615, *Electrostatic discharge sensitivity testing – Transmission line pulse (TLP) – Component level*

3 Terms, definitions, abbreviated terms and conventions

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at http://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

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3.1.1
pulse
abrupt variation of short duration of a physical quantity followed by a rapid return to the initial value

Note 1 to entry: In this document, a pulse can be represented by a voltage or current quantity.

[SOURCE: IEC 60050-161:1990, 161-02-02, modified – Note 1 has been added.]

3.1.2
non-linear
qualifies a circuit (element) for which not all relations between the integral quantities are linear

[SOURCE: IEC 60050-131:2002, 131-11-19]

3.1.3
network
set of ideal circuit elements and their interconnections, considered as a whole

[SOURCE: IEC 60050-131:2002, 131-13-03, modified – The words "in network topology" have been removed at the beginning of the definition as well as the note.]

3.1.4
branch
subset of a network, considered as a two-terminal circuit, consisting of a circuit element or a combination of circuit elements

[SOURCE: IEC 60050-131:2002, 131-13-06]

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3.1.5
node
end-point of a branch connected or not to one or more other branches

[SOURCE: IEC 60050:2002, 131-13-07, modified – The US term "vertex" has been removed.]

3.1.6
external terminal
terminal of an integrated circuit macro-model which interfaces the model to the external environment of the integrated circuit

EXAMPLE Power supply pins and input/output pins.

[SOURCE: IEC 62433-2:2017, 3.1.1, modified – The note has been removed.]

3.1.7
internal terminal
terminal of an integrated circuit macro-model's component which interfaces the component to other components of the integrated circuit macro-model

[SOURCE: IEC 62433-2:2017, 3.1.2, modified – The note has been removed.]

3.1.8
performance degradation
undesired deviation in the operational performance of any device, equipment or system from its intended performance

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Note 1 to entry: The term "degradation" can apply to both recoverable failure and permanent silicon damage.

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3.1.9
hard failure
irreversible failure due to damage of the IC

3.1.10
soft failure
temporary functional failure, self or user recoverable

3.1.11
PPN
Pulse Propagation Network
electrical network that models the propagation network of the disturbance

3.1.12
PDN
Passive Distribution Network
the part of the PPN that represents the linear characteristics of propagation path of electromagnetic noises such as power distribution network

[SOURCE: IEC 62433-2:2017, 3.1.10, modified – The definition has been adapted to linear part of the PPN.]

3.1.13
DI
Disturbance Input
input terminal for the injection of transient disturbances

Note 1 to entry: It could be any pin of IC, an input, supply or an output.