



SLOVENSKI STANDARD
SIST EN 300 417-3-2 V1.1.2:2003
01-december-2003

DfYbcg]b`a i `hjd`Y_g]fUb`Y`fHAŁĚ; YbYf] bY`nU hYj Y`nUdfYbcgbc`Z b_V]cbUbcgh
cdfYa YĚ' !&"XY. : i b_V]Y`d`Ugh]fY[YbYfUrcfg_Y[U]b`a i `hjd`Y_gbY[UcXgY_U`nU
g]b\ fcb]dfYbcgb]a cXi `!B`fGHA!BŁĚDfcZcfa UgdYV]Z_UW]U]n`Uj Y`c`g`UXbcgh]
]nj YXVYf7 GL

Transmission and Multiplexing (TM); Generic requirements of transport functionality of
equipment; Part 3-2: Synchronous Transport Module-N (STM-N) regenerator and
multiplex section layer functions; Implementation Conformance Statement (ICS)
proforma specification

STANDARD PREVIEW
(standards.iteh.ai)

<https://standards.iteh.ai/catalog/standards/sist/28de2cc4-dbaf-46dc-bd6c-e9aafaac55c5/sist-en-300-417-3-2-v1-1-2-2003>

Ta slovenski standard je istoveten z: EN 300 417-3-2 Version 1.1.2

ICS:

33.040.20 Prenosni sistem Transmission systems

SIST EN 300 417-3-2 V1.1.2:2003 en

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN 300 417-3-2 V1.1.2:2003

<https://standards.iteh.ai/catalog/standards/sist/28de2cc4-dba4-46dc-bd6c-e9aafaac55c5/sist-en-300-417-3-2-v1-1-2-2003>

EN 300 417-3-2 V1.1.2 (1998-11)

European Standard (Telecommunications series)

**Transmission and Multiplexing (TM);
Generic requirements of transport functionality of equipment;
Part 3-2: Synchronous Transport Module-N (STM-N)
regenerator and multiplex section layer functions
Implementation Conformance Statement (ICS)
proforma specification**

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 300 417-3-2 V1.1.2:2003](https://standards.iteh.ai/catalog/standards/sist/28de2cc4-dbaf-46dc-bd6c-e9aafaac55c5/sist-en-300-417-3-2-v1-1-2-2003)

<https://standards.iteh.ai/catalog/standards/sist/28de2cc4-dbaf-46dc-bd6c-e9aafaac55c5/sist-en-300-417-3-2-v1-1-2-2003>



Reference

REN/TM-01015-3-2 (3v0riidc.PDF)

Keywords

ICS, STM, SDH, transmission, testing

ETSI

Postal address

F-06921 Sophia Antipolis Cedex - FRANCE

Office address

650 Route des Lucioles - Sophia Antipolis
Valbonne - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65

47 16

Siret N° 348 623 562 000173 - NAF 742 C 2003

Association à but non lucratif enregistrée à la
Sous-Préfecture de Grasse (06) N° 7803/88

Internet

secretariat@etsi.fr
<http://www.etsi.org>

Copyright Notification

No part may be reproduced except as authorized by written permission.
The copyright and the foregoing restriction extend to reproduction in all media.

© European Telecommunications Standards Institute 1998.
All rights reserved.

Contents

Intellectual Property Rights.....	9
Foreword	9
Introduction	10
1 Scope.....	11
2 References.....	11
3 Definitions and abbreviations	12
3.1 Definitions	12
3.2 Abbreviations.....	12
4 Conformance to this ICS proforma specification	15
Annex A (normative): ICS proforma for EN 300 417-3-1.....	16
A.1 Guidance for completing the ICS proforma.....	16
A.1.1 Purposes and structure	16
A.1.2 Abbreviations and conventions	16
A.1.3 Instructions for completing the ICS proforma	18
Annex B (normative): ICS proforma for STM-1 regenerator section layer	19
B.1 Identification of the implementation.....	19
B.1.1 Date of the statement	19
B.1.2 Implementation Under Test (IUT) identification	19
B.1.3 System Under Test (SUT) identification.....	20
B.1.4 Product supplier.....	20
B.1.5 Client	21
B.1.6 ICS contact person.....	21
B.2 Identification of the EN.....	22
B.3 Global statement of conformance of STM-1 Regenerator Section (RS1) layer	22
B.4 RS1 Layer function	23
B.4.1 RS1 layer description.....	23
B.4.2 RS1 layer transmission tables	24
B.4.2.1 RS1 connection function: RS1_C.....	24
B.4.2.2 STM-1 regenerator section layer trail termination functions: RS1_TT_So and RS1_TT_Sk.....	24
B.4.2.2.1 Frame alignment signal.....	24
B.4.2.2.2 FAS generation	24
B.4.2.2.3 Signal scrambling / descrambling.....	25
B.4.2.2.4 In service error monitoring process	26
B.4.2.2.5 Trail Trace Identifier (TTI)	27
B.4.2.3 RS1 layer to MS1 Layer adaptation functions: RS1/MS1_A_So and RS1/MS1_A_Sk.....	29
B.4.2.3.1 RS1 layer to STM-1 Multiplex Section (MS1) layer multiplexing and demultiplexing processes	29
B.4.2.4 RS1 layer to DCC Layer adaptation functions: RS1/DCC_A_So and RS1/DCC_A_Sk.....	29
B.4.2.4.1 RS1 layer to DCC layer multiplexing and demultiplexing processes	29
B.4.2.5 RS1 layer to P0s layer adaptation functions: RS1/P0s_A_So-N and RS1/P0s_A_Sk-N.....	30
B.4.2.5.1 RS1 layer to P0s layer multiplexing and demultiplexing processes.....	30
B.4.2.5.2 RS1 layer to P0s layer frequency justification and bitrate adaptation processes	30
B.4.2.6 RS1 layer to V0x layer adaptation functions: RS1/V0x_A_So and RS1/V0x_A_Sk.....	31
B.4.2.6.1 RS1 layer to V0x layer multiplexing and demultiplexing processes.....	31
B.4.3 Defect, fault and performance monitoring	32
B.4.3.1 Trail termination point mode management.....	32
B.4.3.2 Defect detection and clearance criteria.....	32
B.4.3.3 Consequent action activation and clearance criteria.....	33

B.4.3.4	Defect correlation.....	34
Annex C (normative): ICS proforma for STM-1 multiplex section layer		35
C.1	Identification of the implementation.....	35
C.1.1	Date of the statement	35
C.1.2	Implementation Under Test (IUT) identification	35
C.1.3	System Under Test (SUT) identification.....	35
C.1.4	Product supplier	36
C.1.5	Client	36
C.1.6	ICS contact person.....	37
C.2	Identification of the EN.....	37
C.3	Global statement of conformance of MS1 layer	37
C.4	MS1 section layer function	38
C.4.1	MS1 layer description.....	38
C.4.2	MS1 layer transmission tables	40
C.4.2.1	MS1 connection function: MS1_C.....	40
C.4.2.2	MS1 layer trail termination functions: MS1_TT_So and MS1_TT_Sk	41
C.4.2.2.1	In service error monitoring process	41
C.4.2.2.2	Server layer status monitoring process	42
C.4.2.2.2.1	MS1 Alarm Indication Signal (MS1 AIS).....	42
C.4.2.2.3	Remote indicators monitoring process.....	42
C.4.2.2.3.1	MS1 Remote Defect Indication (MS1 RDI).....	42
C.4.2.2.3.2	MS1 Remote Error Indication (REI) (MS1 REI).....	43
C.4.2.3	MS1 layer to S4 layer adaptation functions: MS1/S4_A_So and MS1/S4_A_Sk.....	44
C.4.2.3.1	MS1 layer to S4 Layer frequency justification and bitrate adaptation processes.....	44
C.4.2.3.2	MS1 layer to S4 layer alignment process.....	45
C.4.2.3.2.1	AU-4 pointer generation	47
C.4.2.3.2.2	AU-4 pointer interpretation.....	50
C.4.2.3.3	MS1 layer to S4 layer multiplexing and demultiplexing processes	54
C.4.2.4	MS1 layer to DCC layer adaptation functions: MS1/DCC_A_So and MS1/DCC_A_Sk.....	55
C.4.2.4.1	MS1 layer to DCC layer multiplexing and demultiplexing processes	55
C.4.2.5	MS1 layer to P0s layer adaptation functions: MS1/P0s_A_So and MS1/P0s_A_Sk.....	55
C.4.2.5.1	MS1 layer to P0s layer frequency justification and bitrate adaptation processes	55
C.4.2.5.2	MS1 layer to P0s layer multiplexing and demultiplexing processes.....	56
C.4.3	MS1 linear trail protection transmission tables.....	57
C.4.3.1	MS1 linear trail protection connection functions: MS1P1+1_C and MS1P1:n_C.....	59
C.4.3.2	MS1 linear protection trail termination functions: MS1P_TT_So and MS1P_TT_Sk.....	60
C.4.3.3	MS1 linear trail protection adaptation functions: MS1/MS1P_A_So and MS1/MS1P_A_Sk.....	61
C.4.3.3.1	MS1 layer to MS1 protection layer multiplexing and demultiplexing processes.....	61
C.4.3.4	MS1 linear trail protection processes	61
C.4.3.4.1	Automatic Protection Switching (APS) externally initiated commands.....	61
C.4.3.4.2	Automatic Protection Switching (APS) automatically initiated commands.....	63
C.4.3.4.3	Automatic Protection Switching (APS) generalities.....	64
C.4.3.4.4	Automatic Protection Switching (APS) switch performance	65
C.4.3.4.5	Automatic Protection Switching (APS) subprocesses.....	65
C.4.3.4.6	Automatic Protection Switching (APS) signal generation	67
C.4.3.4.7	Automatic Protection Switching (APS) signal interpretation	68
C.4.3.4.8	Automatic Protection Switching (APS) status report.....	69
C.4.4	MS1 layer defect, fault and performance monitoring tables	69
C.4.4.1	Port status management.....	69
C.4.4.2	Defect detection and clearance criteria.....	70
C.4.4.3	Consequent action activation and clearance criteria.....	72
C.4.4.4	Defect correlation.....	74
C.4.4.5	Performance monitoring.....	75
C.4.4.5.1	Near end performance monitoring.....	75
C.4.4.5.2	Far end performance monitoring	75
C.4.4.5.3	Pointer performance monitoring.....	76
C.4.5	MS1 protection layer defect, fault and performance monitoring tables	76

C.4.5.1	Defect detection and clearance criteria.....	76
C.4.5.2	Consequent action activation and clearance criteria.....	78
C.4.5.3	Defect correlation.....	79
C.4.5.4	Performance monitoring.....	80

Annex D (normative): ICS proforma for STM-4 regenerator section layer81

D.1	Identification of the implementation.....	81
D.1.1	Date of the statement	81
D.1.2	Implementation Under Test (IUT) identification	81
D.1.3	System Under Test (SUT) identification.....	81
D.1.4	Product supplier	82
D.1.5	Client	82
D.1.6	ICS contact person.....	83
D.2	Identification of the EN.....	83
D.3	Global statement of conformance of RS-4 regenerator section (RS4).....	83
D.4	RS4 section layer function	84
D.4.1	STM-4 regenerator section layer description.....	84
D.4.2	RS-4 regenerator section Layer Transmission Tables.....	85
D.4.2.1	RS-4 regenerator section connection function: RS4_C	85
D.4.2.2	RS-4 regenerator section layer trail termination functions: RS4_TT_So and RS4_TT_Sk	85
D.4.2.2.1	FAS.....	85
D.4.2.2.2	FAS generation	85
D.4.2.2.3	Signal scrambling / descrambling	86
D.4.2.2.4	In service error monitoring process	87
D.4.2.2.5	Trail Trace Identifier (TTI)	88
D.4.2.3	STM-4 regenerator section layer to MS4 layer adaptation functions: RS4/MS4_A_So and RS4/MS4_A_Sk.....	90
D.4.2.3.1	RS4 layer to MS4 layer multiplexing and demultiplexing processes.....	90
D.4.2.4	STM-4 regenerator section layer to DCC layer adaptation functions: RS4/DCC_A_So and RS4/DCC_A_Sk.....	90
D.4.2.4.1	RS4 layer to DCC layer multiplexing and demultiplexing processes	90
D.4.2.5	STM-4 regenerator section layer to P0s layer adaptation functions: RS4/P0s_A_So-N and RS4/P0s_A_Sk-N.....	91
D.4.2.5.1	RS4 layer to P0s layer multiplexing and demultiplexing processes.....	91
D.4.2.5.2	RS4 layer to P0s layer frequency justification and bitrate adaptation processes	91
D.4.2.6	STM-4 regenerator section layer to V0x layer adaptation functions: RS4/V0x_A_So and RS4/V0x_A_Sk.....	92
D.4.2.6.1	RS4 layer to V0x layer multiplexing and demultiplexing processes.....	92
D.4.3	Defect, fault and performance monitoring	93
D.4.3.1	Trail termination point mode management.....	93
D.4.3.2	Defect detection and clearance criteria.....	93
D.4.3.3	Consequent action activation and clearance criteria.....	94
D.4.3.4	Defect correlation.....	95

Annex E (normative): ICS proforma for STM-4 multiplex section layer96

E.1	Identification of the implementation.....	96
E.1.1	Date of the statement	96
E.1.2	Implementation Under Test (IUT) identification	96
E.1.3	System Under Test (SUT) identification.....	96
E.1.4	Product supplier	97
E.1.5	Client	97
E.1.6	ICS contact person.....	98
E.2	Identification of the EN.....	98
E.3	Global statement of conformance of STM-4 Multiplex Section (MS4) layer	98
E.4	MS4 layer function.....	99
E.4.1	MS4 layer Description	99

E.4.2	MS4 layer transmission tables	101
E.4.2.1	MS4 connection function: MS4_C	102
E.4.2.2	MS4 layer trail termination functions: MS4_TT_So and MS4_TT_Sk	102
E.4.2.2.1	In service error monitoring process	102
E.4.2.2.2	Server layer status monitoring process	103
E.4.2.2.2.1	MS4 Alarm Indication Signal (MS4 AIS)	103
E.4.2.2.3	Remote indicators monitoring process	103
E.4.2.2.3.1	MS4 Remote Defect Indication (RDI) (MS4 RDI)	103
E.4.2.2.3.2	MS4 Remote Error Indication (REI) (MS4 REI)	104
E.4.2.3	MS4 layer to S4 layer adaptation functions: MS4/S4_A_So and MS4/S4_A_Sk	105
E.4.2.3.1	MS4 layer to S4 layer frequency justification and bitrate adaptation processes	106
E.4.2.3.2	MS4 layer to S4 layer alignment process	106
E.4.2.3.2.1	AU pointer generation	108
E.4.2.3.2.2	AU pointer interpretation	111
E.4.2.3.3	MS4 layer to S4 layer multiplexing and demultiplexing processes	116
E.4.2.4	MS4 layer to S4-4c layer adaptation functions: MS4/S4-4c_A_So and MS4/S4-4c_A_Sk	116
E.4.2.4.1	MS4 layer to S4-4c layer frequency justification and bitrate adaptation processes	117
E.4.2.4.2	MS4 layer to S4-4c layer alignment process	117
E.4.2.4.2.1	Concatenation indicator recovery process	119
E.4.2.4.3	MS4 layer to S4-4c layer multiplexing and demultiplexing processes	121
E.4.2.5	MS4 layer to DCC Layer adaptation functions: MS4/DCC_A_So and MS4/DCC_A_Sk	121
E.4.2.5.1	MS4 layer to DCC layer multiplexing and demultiplexing processes	121
E.4.2.6	MS4 layer to P0s layer adaptation functions: MS4/P0s_A_So and MS4/P0s_A_Sk	122
E.4.2.6.1	MS4 layer to P0s layer frequency justification and bitrate adaptation processes	122
E.4.2.6.2	MS4 layer to P0s layer multiplexing and demultiplexing processes	122
E.4.3	MS4 Linear Trail Protection Transmission Tables	123
E.4.3.1	MS4 Linear Trail Protection Connection Functions: MS4P1+L_C and MS4P1:n_C	125
E.4.3.2	MS4 Linear Trail Protection Trail Termination Functions: MS4P_TT_So and MS4P_TT_Sk	126
E.4.3.3	MS4 Linear Trail Protection Adaptation Functions: MS4/MS4P_A_So and MS4/MS4P_A_Sk	127
E.4.3.3.1	MS4 layer to MS4 Protection layer multiplexing and demultiplexing processes	127
E.4.3.4	MS4 Linear Trail Protection processes	127
E.4.3.4.1	Automatic Protection Switching (APS) externally initiated commands	127
E.4.3.4.2	Automatic Protection Switching (APS) automatically initiated commands	129
E.4.3.4.3	Automatic Protection Switching (APS) generalities	130
E.4.3.4.4	Automatic Protection Switching (APS) switch performance	131
E.4.3.4.5	Automatic Protection Switching (APS) subprocesses	131
E.4.3.4.6	Automatic Protection Switching (APS) signal generation	133
E.4.3.4.7	Automatic Protection Switching (APS) signal interpretation	134
E.4.3.4.8	Automatic Protection Switching (APS) status report	135
E.4.4	MS4 layer defect, fault and performance monitoring tables	135
E.4.4.1	Port status management	135
E.4.4.2	Defect detection and clearance criteria	136
E.4.4.3	Consequent action activation and clearance criteria	139
E.4.4.4	Defect correlation	142
E.4.4.5	Performance monitoring	143
E.4.4.5.1	Near end performance monitoring	143
E.4.4.5.2	Far end performance monitoring	143
E.4.4.5.3	Pointer performance monitoring	144
E.4.5	MS4 linear trail protection defect, fault and performance monitoring tables	144
E.4.5.1	Defect detection and clearance criteria	144
E.4.5.2	Consequent action activation and clearance criteria	146
E.4.5.3	Defect correlation	147
E.4.5.4	Performance monitoring	148

Annex F (normative): ICS proforma for STM-16 regenerator section layer149

F.1	Identification of the implementation	149
F.1.1	Date of the statement	149
F.1.2	Implementation Under Test (IUT) identification	149
F.1.3	System Under Test (SUT) identification	149
F.1.4	Product supplier	150

F.1.5	Client	150
F.1.6	ICS contact person	151
F.2	Identification of the EN	151
F.3	Global statement of conformance of STM-16 Regenerator Section (RS16) layer	151
F.4	RS16 Section Layer function	152
F.4.1	RS16 layer description	152
F.4.2	STM-16 regenerator section layer transmission tables	153
F.4.2.1	STM-16 Regenerator section connection function: RS16_C	153
F.4.2.2	RS16 layer trail termination functions: RS16_TT_So and RS16_TT_Sk	153
F.4.2.2.1	FAS	153
F.4.2.2.2	Frame Alignment Signal generation	153
F.4.2.2.3	Signal scrambling / descrambling	154
F.4.2.2.4	In service error monitoring process	155
F.4.2.2.5	Trail Trace Identifier (TTI)	156
F.4.2.3	STM-16 regenerator section layer to MS16 Layer adaptation functions: RS16/MS16_A_So and RS16/MS16_A_Sk	158
F.4.2.3.1	RS16 layer to MS16 layer multiplexing and demultiplexing processes	158
F.4.2.4	RS16 layer to DCC layer adaptation functions: RS16/DCC_A_So and RS16/DCC_A_Sk	158
F.4.2.4.1	RS16 layer to DCC layer multiplexing and demultiplexing processes	158
F.4.2.5	RS16 layer to P0s layer adaptation functions: RS16/P0s_A_So-N and RS16/P0s_A_Sk-N	159
F.4.2.5.1	RS16 layer to P0s layer multiplexing and demultiplexing processes	159
F.4.2.5.2	RS16 layer to P0s layer frequency justification and bitrate adaptation processes	159
F.4.2.6	RS16 layer to V0x layer adaptation functions: RS16/V0x_A_So and RS16/V0x_A_Sk	160
F.4.2.6.1	RS16 layer to V0x layer multiplexing and demultiplexing processes	160
F.4.3	Defect, fault and performance monitoring	161
F.4.3.1	Trail termination point mode management	161
F.4.3.2	Defect detection and clearance criteria	161
F.4.3.3	Consequent action activation and clearance criteria	162
F.4.3.4	Defect correlation	163
STANDARD PREVIEW (standards.iteh.ai)SIST EN 300 417-3-2 V1.1.2:2003		
Annex G (normative):	ICS proforma for STM-16 multiplex section layer	164
G.1	Identification of the implementation	164
G.1.1	Date of the statement	164
G.1.2	Implementation Under Test (IUT) identification	164
G.1.3	System Under Test (SUT) identification	164
G.1.4	Product supplier	165
G.1.5	Client	165
G.1.6	ICS contact person	166
G.2	Identification of the EN	166
G.3	Global statement of conformance of STM-16 Multiplex Section (MS16) layer	166
G.4	MS16 Section Layer function	167
G.4.1	MS16 layer description	167
G.4.2	MS16 layer transmission tables	171
G.4.2.1	MS16 connection function: MS16_C	171
G.4.2.2	MS16 layer trail termination functions: MS16_TT_So and MS16_TT_Sk	172
G.4.2.2.1	In service error monitoring process	172
G.4.2.2.2	Server layer status monitoring process	173
G.4.2.2.2.1	MS16 Alarm Indication Signal (MS16 AIS)	173
G.4.2.2.3	Remote indicators monitoring process	173
G.4.2.2.3.1	MS16 Remote Defect Indication (RDI) (MS16 RDI)	173
G.4.2.2.3.2	MS16 Remote Error Indication (REI) (MS16 REI)	174
G.4.2.3	MS16 layer to S4 layer adaptation functions: MS16/S4_A_So and MS16/S4_A_Sk	175
G.4.2.3.1	MS16 layer to S4 layer frequency justification and bitrate adaptation processes	177
G.4.2.3.2	MS16 layer to S4 layer alignment process	177
G.4.2.3.2.1	AU pointer generation	179
G.4.2.3.2.2	AU pointer interpretation	182

G.4.2.3.3	MS16 layer to S4 layer multiplexing and demultiplexing processes	187
G.4.2.4	MS16 layer to S4-4c layer adaptation functions: MS16/S4-4c_A_So and MS16/S4-4c_A_Sk.....	187
G.4.2.4.1	MS16 layer to S4-4c layer frequency justification and bitrate adaptation processes.....	188
G.4.2.4.2	MS16 layer to S4-4c layer alignment process.....	188
G.4.2.4.2.1	Concatenation indicator recovery process.....	191
G.4.2.4.3	MS16 layer to S4-4c layer multiplexing and demultiplexing processes	193
G.4.2.5	MS16 layer to DCC layer adaptation functions: MS16/DCC_A_So and MS16/DCC_A_Sk.....	193
G.4.2.5.1	MS16 layer to DCC layer multiplexing and demultiplexing processes	193
G.4.2.6	STM-16 Multiplex section layer to P0s layer adaptation functions: MS16/P0s_A_So and MS16/P0s_A_Sk.....	194
G.4.2.6.1	MS16 layer to P0s layer frequency justification and bitrate adaptation processes	194
G.4.2.6.2	MS16 layer to P0s layer multiplexing and demultiplexing processes.....	194
G.4.3	MS16 linear trail protection transmission tables.....	195
G.4.3.1	MS16 linear trail protection connection functions: MS16P1+1_C and MS16P1:n_C.....	197
G.4.3.2	MS16 linear protection trail termination functions: MS16P_TT_So and MS16P_TT_Sk.....	198
G.4.3.3	MS16 linear trail protection adaptation functions: MS16/MS16P_A_So and MS16/MS16P_A_Sk.....	199
G.4.3.3.1	MS16 layer to MS16 protection layer multiplexing and demultiplexing processes.....	199
G.4.3.4	MS16 linear trail protection processes	199
G.4.3.4.1	Automatic Protection Switching (APS) externally initiated commands.....	199
G.4.3.4.2	Automatic Protection Switching (APS) automatically initiated commands.....	200
G.4.3.4.3	Automatic Protection Switching (APS) generalities	202
G.4.3.4.4	Automatic Protection Switching (APS) switch performance	202
G.4.3.4.5	Automatic Protection Switching (APS) subprocesses.....	202
G.4.3.4.6	Automatic Protection Switching (APS) signal generation	204
G.4.3.4.7	Automatic Protection Switching (APS) signal interpretation	205
G.4.3.4.8	Automatic Protection Switching (APS) status report.....	206
G.4.4	MS16 two-fibre shared protection ring transmission tables.....	206
G.4.4.1	MS16 two-fibre shared protection ring connection functions: MS16P2fsh_C.....	208
G.4.4.2	MS16 two-fibre Shared Protection Ring trail termination functions: MS16P2fsh_TT_So and MS16P2fsh_TT_Sk.....	209
G.4.4.3	MS16 to MS16 two-fibre Shared Protection Ring adaptation functions: MS16/MS16P2fsh_A_So and MS16/MS16P2fsh_A_Sk.....	210
G.4.3.3.1	MS16 to MS16 two-fibre Shared Protection Ring multiplexing and demultiplexing processes	210
G.4.4.4	MS16 two-fibre shared protection ring processes	211
G.4.4.4.1	Automatic Protection Switching (APS) externally initiated commands.....	211
G.4.4.4.2	Automatic Protection Switching (APS) automatically initiated commands.....	212
G.4.4.4.3	Ring node Automatic Protection Switching (APS) generalities.....	213
G.4.4.4.4	Ring node Automatic Protection Switching (APS) states	213
G.4.4.4.5	Ring node Automatic Protection Switching (APS) state transitions	216
G.4.5	MS16 layer defect, fault and performance monitoring tables	221
G.4.5.1	Port status management.....	221
G.4.5.2	Defect detection and clearance criteria.....	221
G.4.5.3	Consequent action activation and clearance criteria.....	224
G.4.5.4	Defect correlation.....	227
G.4.5.5	Performance monitoring.....	228
G.4.5.5.1	Near end performance monitoring.....	228
G.4.5.5.2	Far end performance monitoring	228
G.4.5.5.3	Pointer performance monitoring	229
G.4.6	MS16 linear trail protection defect, fault and performance monitoring tables.....	229
G.4.6.1	Defect detection and clearance criteria.....	229
G.4.6.2	Consequent action activation and clearance criteria.....	231
G.4.6.3	Defect correlation.....	232
G.4.6.4	Performance monitoring.....	233
G.4.7	MS16 two-fibre shared protection ring defect, fault and performance monitoring tables.....	233
G.4.7.1	Defect detection and clearance criteria.....	233
G.4.7.2	Consequent action activation and clearance criteria.....	233
G.4.7.3	Defect correlation.....	235
G.4.7.4	Performance monitoring.....	235
History		236

Intellectual Property Rights

IPRs essential or potentially essential to the present document may have been declared to ETSI. The information pertaining to these essential IPRs, if any, is publicly available for **ETSI members and non-members**, and can be found in SR 000 314: *"Intellectual Property Rights (IPRs); Essential, or potentially Essential, IPRs notified to ETSI in respect of ETSI standards"*, which is available **free of charge** from the ETSI Secretariat. Latest updates are available on the ETSI Web server (<http://www.etsi.org/ipr>).

Pursuant to the ETSI IPR Policy, no investigation, including IPR searches, has been carried out by ETSI. No guarantee can be given as to the existence of other IPRs not referenced in SR 000 314 (or the updates on the ETSI Web server) which are, or may be, or may become, essential to the present document.

Foreword

This European Standard (Telecommunications series) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

The present document is one of a family of documents that has been produced in order to provide inter-vendor and inter-operator compatibility of Synchronous Digital Hierarchy (SDH) equipment.

The present document is part 3-2 of a multi-part EN covering the Generic requirements of transport functionality of equipment, as identified below:

Part 1-1: "Generic processes and performance".

Part 1-2: "General information about Implementation Conformance Statement (ICS) proforma".

Part 1-3 "Generic processes and performance; Abstract Test Suite (ATS)".

Part 2-1: "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions".

Part 2-2: "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 2-3: "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions; Abstract Test Suite (ATS)".

Part 3-1: "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".

Part 3-2: "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 3-3: "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions; Abstract Test Suite (ATS)".

Part 4-1: "Synchronous Digital Hierarchy (SDH) path layer functions".

Part 4-2: "Synchronous Digital Hierarchy (SDH) path layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 4-3: "Synchronous Digital Hierarchy (SDH) path layer functions; Abstract Test Suite (ATS)".

Part 5-1: "Plesiochronous Digital Hierarchy (PDH) path layer functions".

Part 5-2: "Plesiochronous Digital Hierarchy (PDH) path layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 5-3: "Plesiochronous Digital Hierarchy (PDH) path layer functions; Abstract Test Suite (ATS)".

Part 6-1: "Synchronization layer functions".

Part 6-2: "Synchronization layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 6-3: "Synchronization layer functions; Abstract Test Suite (ATS)".

Part 7-1: "Auxiliary layer functions".

Part 7-2: "Auxiliary layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 7-3: "Auxiliary layer functions; Abstract Test Suite (ATS)".

Parts 2 to 7 specify the layers and their atomic functions.

NOTE 1: The present document does not currently address configuration management.

NOTE 2: The SDH radio equipment functional blocks are addressed by ETSI WG TM4.

Various of the above parts have previously been published as parts of EN 300 417.

They have been converted to parts of EN 300 417 without technical changes, but some editorial changes have been necessary (e.g. references). In particular:

- Parts 2-1 and 3-2 have been modified to take account of editorial errors present in edition 1.
- Part 1-1 has had its title change of to align with other parts published at a later date.

Also note that in the meantime parts 8-1, 8-2 and 8-3 have been stopped.

Proposed national transposition dates	
Date of adoption of this EN:	24 October 1997
Date of latest announcement of this EN (doa):	28 February 1998
Date of latest publication of new National Standard or endorsement of this EN (dop/e):	31 August 1998
Date of withdrawal of any conflicting National Standard (dow):	31 August 1998

Introduction

To evaluate conformance of a particular implementation, it is necessary to have a statement of which capabilities and options have been implemented for a telecommunication specification. Such a statement is called an Implementation Conformance Statement (ICS).

A client of a test laboratory who requests a conformance / approval test shall provide to the test laboratory a completed ICS proforma for each layer to be tested and a detailed system description of the implementation.

The ICS proforma is not another complete description of the related specification, but rather a compact form of its static conformance requirements, to be used by the test laboratory to identify which test shall be performed on a given implementation. Not every feature of a profile specification is contained in the related ICS proforma. For particular cases requiring specific information the ICS can refer to the appropriate clause of the related specification by means of references, notes and or comments.

The ICS proforma captures the implementation flexibility allowed by the related specification and details which option are left to the implementor, which are conditionally dependent on other option taken by the implementor.

1 Scope

The present document provides the Implementation Conformance Statement (ICS) proforma specification for the Synchronous Transport Module-1 (STM-1), STM-4 and STM-16 regenerator section and multiplex section layer functions defined in EN 300 417-3-1 [2] in compliance with the relevant requirements, and in accordance with the relevant guidance given in ISO/IEC 9646-7 [7] and ETS 300 406 [3].

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

- [1] EN 300 417-1-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 1-1: Generic processes and performance".
- [2] EN 300 417-3-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 3-1: Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".
- [3] ETS 300 406 (1995): "Methods for testing and Specification (MTS); Protocol and profile conformance testing specifications; Standardization methodology".
- [4] ETS 300 232: "Transmission and Multiplexing (TM); Optical interfaces for equipments and systems relating to the Synchronous Digital Hierarchy [ITU-T Recommendation G.957 (1993) modified]".
- [5] ITU-T Recommendation G.957 (1995): "Optical interfaces for equipments and systems relating to the synchronous digital hierarchy".
- [6] ISO/IEC 9646-1 (1994): "Information technology; Open systems interconnection; Conformance testing methodology and framework; Part 1: General concepts".
- [7] ISO/IEC 9646-7 (1995): "Information technology; Open systems interconnection; Conformance testing methodology and framework; Part 7: Implementation Conformance Statements".
- [8] ETS 300 147 (1992): "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Multiplexing structure".
- [9] CCITT Recommendation G.704 (1991): "Synchronous frame structures used at primary and secondary hierarchical levels".
- [10] CCITT Recommendation G.751 (1988): "Digital multiplex equipments operating at third order bit rate of 34 368 kbit/s and fourth order bit rate of 139 264 kbit/s and using positive justification".
- [11] ITU-T Recommendation G.823 (1993): "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".
- [12] ITU-T Recommendation G.825 (1993): "The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)".

- [13] ITU-T Recommendation G.826 (1993): "Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate".
- [14] ITU-T Recommendation G.707 (1996): "Network node interface for the Synchronous Digital Hierarchy (SDH)".
- [15] ETS 300 746 (1997): "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Network protection schemes; Automatic Protection Switch (APS) protocols and operation".
- [16] TS 101 009: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Network Protection schemes; Types and characteristics".
- [17] EN 300 417-2-2: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 2-2: Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions; Implementation Conformance Statement (ICS) proforma specification".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following definitions apply:

- terms defined in EN 300 417-3-1 [2];
- terms defined in ISO/IEC 9646-1 [6] and in ISO/IEC 9646-7 [7].

In particular, the following terms defined in ISO/IEC 9646-1 [6] apply:

Implementation Conformance Statement (ICS): A statement made by the supplier of an implementation or system claimed to conform to a given specification, stating which capabilities have been implemented. The ICS can take several forms: protocol ICS, profile ICS, profile specific ICS, information object ICS, etc.

ICS proforma: A document, in the form of a questionnaire, which when completed for an implementation or system becomes an ICS.

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

A	Adaptation function
AcTI	Accepted Trace Identifier
ADM	Add-Drop Multiplexer
AI	Adapted Information
AIS	Alarm Indication Signal
AP	Access Point
APId	Access Point Identifier
APS	Automatic Protection Switch
AU	Administrative Unit
AUG	Administrative Unit Group
AU-n	Administrative Unit, level n
BER	Bit Error Rate
BIP	Bit Interleaved Parity
BIP-N	Bit Interleaved Parity, width N
C	Connection function
CI	Characteristic Information
CK	Clock
CM	Connection Matrix

CP	Connection Point
CS	Clock Source
D	Data
DCC	Data Communications Channel
DEC	DECrement
DEG	DEGraded
DEGTHR	DEGraded THReshold
EBC	Errored Block Count
ECC	Embedded Communications Channel
ECC(x)	Embedded Communications Channel, layer x
EDC	Error Detection Code
EDCV	EDC Violation
EMF	Equipment Management Function (EMF)
EQ	EQuipment
ERSN	External Request Signal Number
ERT	External Request Type
ES	Electrical Section
ES	Errored Second
ExTI	Expected Trace Identifier
F_B	Far-end Block
FAS	Frame Alignment Signal
FOP	Failure Of Protocol
FS	Frame Start signal
GRSN	Global Request Signal Number
GRT	Global Request Type
HO	Higher Order
HOVC	Higher Order Virtual Container
HP	Higher order Path
ICS	Implementation Conformance Statement
ID	IDentifier
IF	In Frame state
INC	INCrement
IUT	Implementation Under Test
LBSN	Local Bridge Signal Number
LC	Link Connection
LO	Lower Order
LOA	Loss Of Alignment; generic for LOF, LOM, LOP
LOF	Loss Of Frame
LOP	Loss Of Pointer
LOS	Loss Of Signal
LOVC	Lower Order Virtual Container
LRSN	Local Request Signal Number
LRT	Local Request Type
LSSN	Local Selector Signal Number
MC	Matrix Connection
MCF	Message Communications Function
MDT	Mean Down Time
mei	maintenance event information
MI	Management Information
MO	Managed Object
MON	Monitored
MP	Management Point
MS	Multiplex Section
MS1	STM-1 Multiplex Section
MS16	STM-16 Multiplex Section
MS4	STM-4 Multiplex Section
MSB	Most Significant Bit
MSOH	Multiplex Section OverHead
MSP	Multiplex Section Protection
MSPG	Multiplex Section Protection Group