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Road vehicles — In-vehicle Ethernet —

Part 2:
Common physical entity requirements

Véhicules routiers — Ethernet automotive —

Partie 2: Exigences de l'entité physique commune

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/ TC 22, Road vehicles, Subcommittee SC 31, Data communication.

A list of all parts in the ISO 21111 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

In general, the Ethernet physical layer requirements are specified in ISO/IEC/IEEE 8802-3:2017. The ISO 21111- series of standards provides supplemental specifications (e.g, wake-up, I/O functionality), which are required for in-vehicle Ethernet applications. In road vehicles, Ethernet networks are used for different purposes requiring different bit-rates. Currently, this standard series specifies the 1-Gbit/s optical and 100 Mbit/s electrical physical layer.

The documents in the ISO 21111- series contain requirement specifications and test methods related to the in-vehicle Ethernet. This includes requirement specifications for physical layer entity (e.g. connectors, PHY implementations) providers, device (e.g. electronic control units, gateway units) suppliers, and system (e.g. network systems) designers. Additionally, there are test methods specified for conformance testing and for interoperability testing.

The structure of the specifications given in this series of documents complies with the Open Systems Interconnection (OSI) reference model specified in ISO/IEC 7498-1[[1]] and ISO/IEC 10731[[2]].

ISO 21111-9 specifies the data link layer requirements and conformance test plan. The requirements and test plan for devices and systems that include bridge functionality are specified in this document.

ISO 21111-10 specifies the application to network layer requirements and test plan. The requirements and test plan for devices and systems that include functionality related with OSI layers from 3 to 7 are specified in this document.

Figure 1 shows the parts of the ISO 21111 standard series and the document structure.

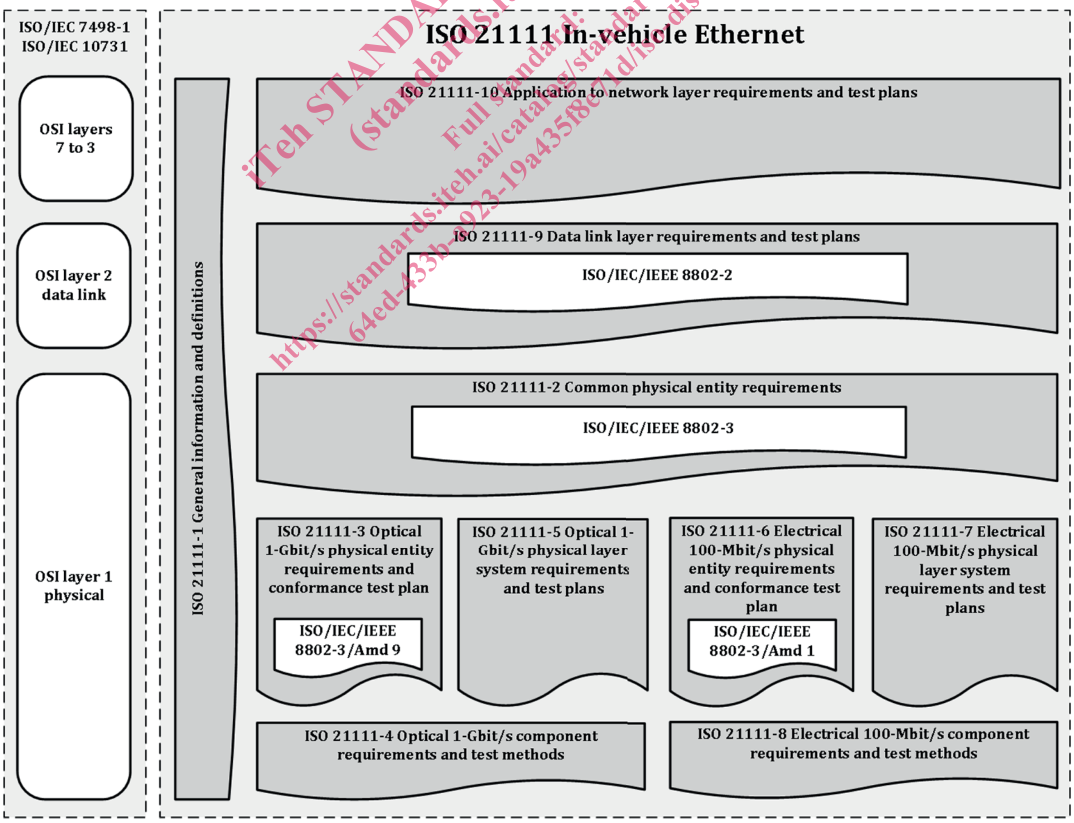
ISO/IEC 7498-1
ISO/IEC 10731
OSI layers 7 to 3
OSI layer 2 data link
OSI layer 1 physical
ISO 21111 In-vehicle Ethernet
ISO 21111-1 General information and definitions
ISO 21111-10 Application to network layer requirements and test plans
ISO 21111-9 Data link layer requirements and test plans
ISO/IEC/IEEE 8802-2
ISO 21111-2 Common physical entity requirements
ISO/IEC/IEEE 8802-3
ISO 21111-3 Optical 1-Gbit/s physical entity requirements and conformance test plan
ISO/IEC/IEEE 8802-3/Amd 9
ISO 21111-5 Optical 1-Gbit/s physical layer system requirements and test plans
ISO 21111-6 Electrical 100-Mbit/s physical entity requirements and conformance test plan
ISO/IEC/IEEE 8802-3/Amd 1
ISO 21111-7 Electrical 100-Mbit/s physical layer system requirements and test plans
ISO 21111-4 Optical 1-Gbit/s component requirements and test methods
ISO 21111-8 Electrical 100-Mbit/s component requirements and test methods

Figure 1 — In-vehicle Ethernet document reference according to the OSI model

Road vehicles — In-vehicle Ethernet —

Part 2:
Common physical entity requirements

1 Scope

This part of ISO 21111 specifies the following items to complement ISO/IEC /IEEE 8802-3:2017.

— Interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII).

— Common physical entity wake-up and synchronized link sleep functionalities independent from physical media and transmission bit rate.

The optical and electrical component requirements and test methods for optical and electrical transmission of in-vehicle Ethernet are not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21111-1:2019, *Road vehicles — In-vehicle Ethernet — Part 1: General information and definitions*

ISO/IEC 7498-1:1994, *Information technology — Open Systems Interconnection — Basic Reference Model: The Basic Model — Part 1*

ISO/IEC/IEEE 8802-3:2017, *Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements — Part 3: Standard for Ethernet*

ISO/IEC 10731:1994, *Information technology — Open Systems Interconnection — Basic Reference Model — Conventions for the definition of OSI services*

JEDEC – JESD8C.01:2006, *Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*

JEDEC – JESD8-5A:2006, *2.5 V ± 0.2 V (Normal Range) and 1.8 V – 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*

JEDEC – JESD8-7A:1997, *1.8 V ± 0.15 V (Normal Range) and 1.2 V – 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*

3 Terms and definitions

3.1
double data rate
DDR
data transmission scheme, in which the data is transferred on both the rising and falling edges of the clock signal

4 Symbols and abbreviated terms

DoD	delay on destination
DoS	delay on source
GMII	gigabit media independent interface
I/O	input and output
MAC	media access control
MDC	management data clock
MDIO	management data input/output
MII	media independent interface
N/A	not applicable
PHY	physical layer
RGMII	reduced gigabit media independent interface
RTBI	reduced ten-bit interface
RX	receiver
TX	transmitter

5 Media independent interfaces

5.1 General

ISO/IEC/IEEE 8802-3:2017 specifies several speed-specific interfaces which are recommended for the communication between the reconciliation sub-layer and the PCS sub-layer. Two of the recommended interfaces are MII, used for10-Mbit/s and 100-Mbit/s capable physical entities, and GMII for 1-Gbit/s capable physical entities.

ISO/IEC/IEEE 8802-3:2017, Clause 22 specifies MII and ISO/IEC/IEEE 8802-3:2017, Clause 35 specifies GMII.

GMII signals, TXD and RXD, as specified in ISO/IEC/IEEE 8802-3:2017, Clause 35 are 8-bits wide. A direct mapping of the TXD or RXD 8-bits wide signals of the GMII interface into eight electrical lines is a drawback for some implementations. A mapping from GMII signals to a reduced set of electrical lines is specified in subclause 5.2.

5.2 RGMII

5.2.1 General

The RGMII architecture (see Figure 2) is composed by the mapping of the GMII interface into a reduced set of signal lines, the reduced set of signal lines, and the de-mapping from the reduced set of signal lines into the GMII interface. In this subclause RGMII signal lines are the reduced set of signal lines in Figure 2.

The RGMII transmitter side adapter shall adapt the GMII signals in the reconciliation sub-layer side to the RGMII signal lines. The RGMII receiver side adapter shall adapt the RGMII signal lines to the GMII signals in the PCS sub-layer side.

Subclause 5.2.2 specifies the RGMII signal lines. Each RGMII signal line is able to transmit an electrical signal. Subclause 5.2.3 specifies the RGMII electrical signal voltage levels and subclause 5.2.4 specifies the RGMII electrical signal timing. Subclause 5.2.5 specifies how the GMII signals shall be mapped to the RGMII signal lines and vice versa.

All signals transmitted in an electrical signal line shall be conveyed with positive logic except as specified differently.

An electrical signal line shall be at logic “high” or “1” when it is at a voltage level greater than certain thereshold. This thereshold depends on the RGMII signal line nominal voltage.

An electrical signal line shall be at logic “low” or “0” when it is at a voltage level lower than certain thereshold. This thereshold depends on the RGMII signal line nominal voltage.

JEDEC - JESD8C.01:2006 specifies the theresholds for RGMII signal line nominal voltage equal to 3,3 V.

JEDEC - JESD8-5A:2006 specifies the theresholds for RGMII signal line nominal voltage equal to 2,5 V.

JEDEC - JESD8-7A:1997 specifies the theresholds for RGMII signal line nominal voltage equal to 1,8 V.

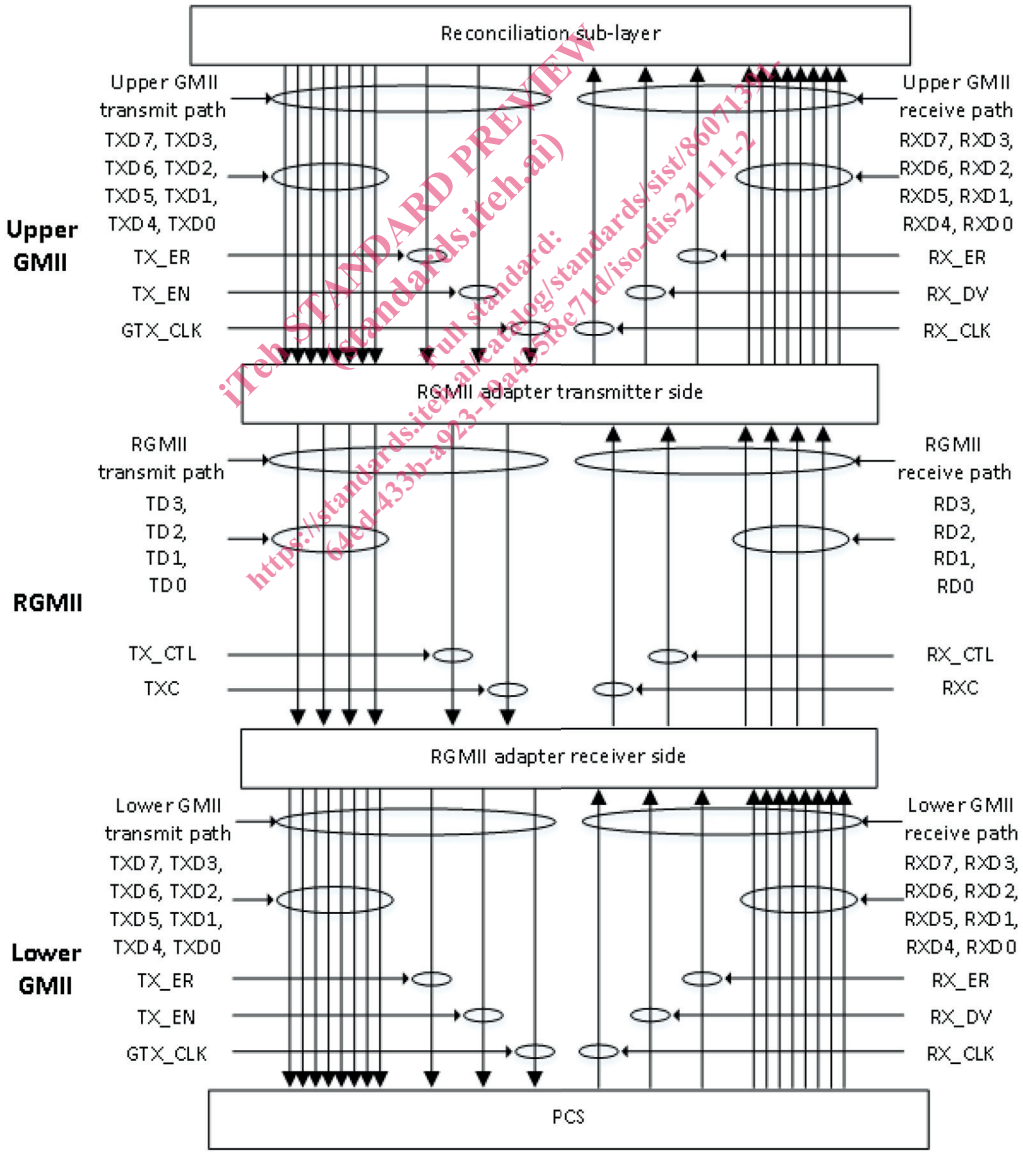

Figure 2 — RGMII architecture

5.2.2 RGMII signals

Figure 2 shows the architecture of the RGMII interface.

The RGMII is a full-duplex bidirectional interface and transfers data simultaneously in both directions. The RGMII connects the upper GMII and the lower GMII interfaces by means of adapters, which convert GMII signals to RGMII signals and vice versa.

The signals of each of the interfaces are grouped by the signal flow direction. The signals going in the up to down direction in Figure 2 compose the transmit path, and the signals going in the down to up direction compose the receive path. The transmitter side adapter is the signal source in the RGMII transmit path and the receiver side adapter is the signal source in the RGMII receive path.

Table 1 defines the conversion of the GMII signals to the RGMII signals in the transmit path at the the transmit side. The signals in the column “RGMII adapter internal signals” are only available inside the adapter and are used to convert the GMII signals. All GMII electrical signals are only valid during the rising edge of the GTX_CLK signal, whereas the RGMII adapter internal signals are valid during both edges of the A_TXC signal.

Table 1 — Conversion table for adapter at transmit side in transmit path

GMII signal	RGMII adapter internal signal		RGMII signal	Remark
	TXC rising edge	TXC falling edge		
GTX_CLK	A_TXC		TXC	N/A
TX_EN	A_TXEN	N/A	TX_CTL	A_TXEN=TX_EN
TX_ER	N/A	A_TXERR		A_TXERR=TX_EN xor TX_ER
TXD7	N/A	A_TD7	TD3	N/A
TXD6	N/A	A_TD6	TD2	N/A
TXD5	N/A	A_TD5	TD1	N/A
TXD4	N/A	A_TD4	TD0	N/A
TXD3	A_TD3	N/A	TD3	N/A
TXD2	A_TD2	N/A	TD2	N/A
TXD1	A_TD1	N/A	TD1	N/A
TXD0	A_TD0	N/A	TD0	N/A

Table 2 defines the conversion of the RGMII signals to GMII signals in the transmit path at the receiver side. The signals in the column “RGMII adapter internal signal” are only available inside the adapter.

Table 2 — Conversion table for adapter at receiver side in transmit path

RGMII signal	RGMII adapter internal signal		GMII signal	Remark
	TXC rising edge	TXC falling edge		
TXC	A_TXC		GTX_CLK	N/A
TX_CTL	A_TXEN	N/A	TX_EN	TX_EN=A_TXEN
	N/A	A_TXERR	TX_ER	TX_ER=A_TXEN xor A_TXERR
TD3	A_TD3	N/A	TXD3	N/A
	N/A	A_TD7	TXD7	N/A
TD2	A_TD2	N/A	TXD2	N/A
	N/A	A_TD6	TXD6	N/A
TD1	A_TD1	N/A	TXD1	N/A
	N/A	A_TD5	TXD5	N/A
TD0	A_TD0	N/A	TXD0	N/A
	N/A	A_TD4	TXD4	N/A

Table 3 defines the conversion of the GMII signals to RGMII signals in the receive path at the receiver side. The signals in the column “RGMII adapter internal signal” are only available inside the adapter.

Table 3 — Conversion table for adapter at receiver side in receive path

GMII signal	RGMII adapter internal signal		RGMII signal	Remark
	TXC rising edge	TXC falling edge		
RX_CLK	A_RXC		RX_CLK	N/A
RX_DV	A_RXDV	N/A	TX_CTL	A_RXDV=RX_DV
RX_ER	N/A	A_RXERR		A_RXERR=RX_DV xor RX_ER
RXD7	N/A	A_RD7	RD3	N/A
RXD6	N/A	A_RD6	RD2	N/A
RXD5	N/A	A_RD5	RD1	N/A
RXD4	N/A	A_RD4	RD0	N/A
RXD3	A_RD3	N/A	RD3	N/A
RXD2	A_RD2	N/A	RD2	N/A
RXD1	A_RD1	N/A	RD1	N/A
RXD0	A_RD0	N/A	RD0	N/A

Table 4 defines the conversion of the RGMII signals to GMII signals in the receive path at the transmitter side. The signals in the column “RGMII adapter internal signal” are only available inside the adapter.

Table 4 — Conversion table for adapter at transmitter side in receive path

RGMII signal	RGMII adapter internal signal		GMII signal	Remark
	TXC rising edge	TXC falling edge		
RXC	A_TXC		GTX_CLK	N/A
RX_CTL	A_RXDV	N/A	RX_DV	RX_DV=A_RXDV
	N/A	A_RXERR	RX_ER	RX_ER=A_RXDV xor A_RXERR
RD3	A_RD3	N/A	RXD3	N/A
	N/A	A_RD7	RXD7	N/A
RD2	A_RD2	N/A	RXD2	N/A
	N/A	A_RD6	RXD6	N/A
RD1	A_RD1	N/A	RXD1	N/A
	N/A	A_RD5	RXD5	N/A
RD0	A_RD0	N/A	RXD0	N/A
	N/A	A_RD4	RXD4	N/A

5.2.3 Electrical signal voltage level

The RGMII electrical signal nominal voltage level of a RGMII signal line shall be at least one of these values: 1,8 V, 2,5 V or 3,3 V

The 100 % value shown in Figure 3 is the RGMII electrical signal nominal voltage level of a RGMII signal line. All electrical signal voltage levels in this document are scaled with the RGMII electrical signal nominal voltage level.