DRAFT AMENDMENT ISO/IEC 14443-4:2016 DAM 3

ISO/IEC JTC 1/SC 17

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Identification cards — Contactless integrated circuit cards — Proximity cards —

Part 4: **Transmission protocol**

AMENDMENT 3: Dynamic power level management

Cartes d'identification — Cartes à circuit intégré sans contact — Cartes de proximité — Partie 4: Protocole de transmission

AMENDEMENT 3: Gestion dynamique de niveau de puissance iTeh STANDARD PREVIEW

ICS: 35.240.15

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Foreword

This document was prepared by Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and security devices for personal identification*.

A list of all parts in the ISO/IEC 14443- series can be found on the ISO website.

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Identification cards — Contactless integrated circuit cards — Proximity cards —

Part 4: Transmission protocol

AMENDMENT 3: Dynamic power level management

Page 3, Clause 4

Add new abbreviated term after PICC:

"PLI_{CID} Power Level Indication in CID field"

Add new abbreviated term after SYNC:

"t_{PL} Guard time for PCD power level change"

Page 20, 7.3

Replace the end of 1st paragraph "1 byte long INF field that consists of two parts (see Figure 21)" with "1 byte long INF field that consists of three parts (see Figure 21)".

Replace the first dash after the first paragraph with:

- b8 is RFU. <u>ISO/IEC 14443-4:2016/DAmd 3</u> https://standards.iteh.ai/catalog/standards/sist/df95a89f-112a-4373-99c3-
- accel = 120 accel = 120
- b7 codes t_{PL} value. $t_{PL} = 5$ ms if b7 is set to (1)b, otherwise t_{PL} equals the default value specified in ISO/IEC 14443-3, 6.5.2.3.

Replace Figure 21 with:





Page 21, 7.4

...

Replace the whole subclause with:

7.4 Power Level Indication

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In the PROTOCOL state, the PICC may use PLI_{CID} to give power level indication to the PCD and PLI_{CID} shall be coded as specified in <u>Table 3</u> using two bits embedded in the CID field (when present) sent by the PICC (see 7.1.2.2).

A PICC that codes

- PLI_{CID} = (00)b does not provide any received power level indication;
- $PLI_{CID} = (01)b$ indicates the received power level is less than ($H_{LP} + H_{step, max}$) (see ISO/IEC 14443-2XX/Amd3). When receiving $PLI_{CID} = (01)b$, the PCD may increase its field strength in one or several consecutive steps and should not decrease its field strength;
- $PLI_{CID} = (10)b$ indicates the received power level is at least ($H_{LP} + H_{step, max}$), but one step decrease may increase the PICC response time. When receiving $PLI_{CID} = (10)b$, the PCD may decrease its field strength by one step only;
- $PLI_{CID} = (11)b$ indicates the received power level is at least ($H_{LP} + H_{step, max}$), but one step decrease is not expected to increase the PICC response time. When receiving $PLI_{CID} = (11)b$, the PCD may decrease its field strength by one step only.

The PCD may increase its field strength in one or several steps before any SOF or start of communication.

PLI _{CID}	Power level indication
(00)b	No indication for field strength RD PREVIEW
(01)b	Field strength is less than $(H_{LP} + H_{step,max})$
(10)b	Field strength is at least $(H_{LP} + H_{step, max})$ One step decrease may increase the PICC response time
(11)b	Field strength $\frac{160}{15}$ $\frac{1443}{2}$ $\frac{160}{15}$ $\frac{1443}{2}$ $\frac{160}{10}$ $\frac{160}{10}$ $\frac{160}{10}$ $\frac{1443}{10}$ $\frac{160}{10}$

Table 3 — Coding of PLI_{CID}

After receiving the power level indication from the PICC, the PCD may change its magnetic field strength in accordance with the power level indication before sending the next block.

The PCD:

- should not change its magnetic field strength when several PICCs are activated;
- may produce magnetic field strength steps which shall not exceed the maximum field strength factor defined in ISO/IEC 14443-2, 6.2;
- shall produce a stable magnetic field strength for at least t_{PL} between any consecutive two magnetic field strength steps and before sending start of communication or SOF;
- shall respect the most recent t_{PL} value indicated by the PICC by PLI_{ATQ} (see ISO/IEC 14443-3, 6.5.2.3) or by b7 in the INF field of an S(WTX) request (see 7.3), or the default t_{PL} value specified in ISO/IEC 14443-3, 6.5.2.3 as long as no such indication was received.

WARNING — A PCD decreasing the field strength in dynamic situations may cause the PICC to go into the POWER-OFF state. A PCD expecting fast moving PICCs, which is typically the case in payment or ticketing systems should handle Dynamic power level management with special care.

"

Page 55, Annex G

Add the following Annex H after Annex G:

Annex H

(informative)

Examples of PLI_{CID} usage

H.1 PICC response time not depending on field strength

An example of PLI_{CID} settings for a PICC whose response time does not depend on its power level is as shown in Figure H.1.



Figure H.1 — PICC response time not depending on field strength iTeh STANDARD PREVIEW

The PCD should increase its power level if it receives $PLI_{CID} = (01)b$ and may decrease its power level if it receives $PLI_{CID} = (11)b$.

H.2 PICC response time partly depending on field strength

An example of PLI_{CID} settings for a PICC whose response time partly depends on its power level is as shown in Figure H.2.



Figure H.2 — PICC response time partly depending on field strength

The PCD may increase its power level if it receives $PLI_{CID} = (01)b$ and may decrease its power level if it receives $PLI_{CID} = (11)b$.

The PCD may increase or decrease its power level if it receives $PLI_{CID} = (10)b$, therefore a PICC wishing the PCD to increase power level may send $PLI_{CID} = (01)b$ instead of $PLI_{CID} = (10)b$.

H.3 PICC response time always depending on field strength

An example of PLI_{CID} settings for PICC whose response time always depends on its power level is as shown in <u>Figure H.3</u>.

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Figure H.3 — PICC response time always depends on field strength

The PCD may increase its power level if it receives PLI_{CID} = (01)b.

The PCD may increase or decrease its power level if it receives $PLI_{CID} = (10)b$, therefore a PICC wishing the PCD to increase power level may send $PLI_{CID} = (01)b$ instead of $PLI_{CID} = (10)b$.

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