SLOVENSKI STANDARD
SIST EN 16603-20-40:2024

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Vesoljska tehnika - Inženiring ASIC, FPGA in jedra IP

Space engineering - ASIC, FPGA and IP Core engineering

Raumfahrttechnik - ASIC und FPGA Technik

Ingénierie spatiale - Ingénierie des ASIC, FPGA et noyaux de PI

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English version

Space engineering - ASIC, FPGA and IP Core engineering

Ingénierie spatiale - Ingénierie des ASIC, FPGA et noyaux de PI

Raumfahrttechnik - Entwicklung von ASICs, FPGAs und IP-Kernen

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European Foreword

This document (EN 16603-20-40:2023) has been prepared by Technical Committee CEN-CENELEC/TC 5 “Space”, the secretariat of which is held by DIN.

This standard (EN 16603-20-40:2023) originates from ECSS-E-ST-20-40C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by June 2024, and conflicting national standards shall be withdrawn at the latest by June 2024.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a standardization request given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

Introduction

Developing custom designed monolithic integrated circuits such as ASICs or FPGAs, and developing IP Cores, as off-the-shelf Building Blocks for these complex ICs, make certain engineering and technical management activities crucial to the success of these developments.

ECSS-E-ST-20-40 was written in parallel and in co-ordination with the writing ECSS-Q-ST-60-03, by the same ECSS Working Group. These two new and complementary standards cover respectively the engineering and the product assurance requirements to be applied when developing ASICs, FPGAs and IP Cores, and these two new standards together supersede ECSS-Q-ST-60-02C.

The DEVICE qualification status is assessed based on the requirements from both ECSS-E-ST-20-40 and ECSS-Q-ST-60-03. In order for a DEVICE to be qualified and accepted according to ECSS standards, the DEVICE development reviews specified in ECSS-E-ST-20-40 have to be declared successful by the customer engineering and PA responsible persons and project management who monitored the DEVICE development.

1
Scope

This standard specifies a comprehensive set of engineering requirements for the successful development of digital, analogue and mixed analogue-digital signal custom designed integrated circuits, such as application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs) and Intellectual Property Cores (IP Cores), from now on referred to with the single and generic term DEVICEs.

Microelectronics systems created by more than one DEVICE die but that are interconnected and packaged together as a single DEVICE are not considered single monolithic DEVICEs. However ECSS-ST-20-40 is to be applied to (a) the development of each individual monolithic die, (b) also for their integration onto a multi-die single DEVICE considering those dice as IP Cores.

This standard may be tailored for the specific characteristic and constraints of a space project in conformance with ECSS-S-ST-00. A pre-tailoring based on the actual DEVICE type and criticality category of the DEVICE is addressed in clause 5.1.2.

This standard does not cover requirements for the selection, control, procurement or usage of DEVICEs for space projects nor DEVICE ESCC qualification requirements, as those requirements are covered by ECSS-Q-ST-60C EEE components standard and the ESCC generic specification No. 9000 respectively. Nevertheless, this standard contemplates the possibility for the DEVICE to undergo ESCC qualification after the DEVICE customer acceptance as an ECSS qualified DEVICE, and thus a DEVICE ESCC Detail Specification and DEVICE Radiation Test Plan and Report are optional expected outputs.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	*ECSS system – Glossary of terms*
EN 16602-30	ECSS-Q-ST-30	*Space product assurance – Dependability*
EN 16602-40	ECSS-Q-ST-40	*Space product assurance – Safety*
-	ECSS-Q-ST-60-03	*Space product assurance – ASIC, FPGA and IP Core product assurance*

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, in particular the following terms:

1. acceptance;
2. component;
3. customer;
4. engineering model;
5. flight model;
6. informative;
7. maintenance;
8. model;
9. normative;
10. performance;
11. project;
12. requirement;
13. risk;
14. supplier.

NOTE The old term *firmware* is defined in ECSS-S-ST-00-01C, and it is not used in the context of ECSS-E-ST-20--40 because with the emergence of new technologies it is now ambiguous and unnecessary. It is important not to confuse terms like *FPGA*, *FPGA programming file* or *FPGA programming bit stream* with *firmware*.

3.2 Terms specific to the present standard

3.2.1 Application Specific Integrated Circuit

full custom or semi custom designed monolithic integrated circuit

NOTE ASICs can be digital, analogue or a mixed function.

3.2.2 block diagram

abstract graphical presentation of interconnected named boxes or blocks representing an architectural or functional drawing

3.2.3 Building Block

reusable IC design element that implements a self-standing function or group of functions for which ownership rights exist and that has been developed in the context of a specific IC project or technology, without the intention to be shared with third parties for its reuse in other IC projects

NOTE For example, an HDL model such as synthesizable VHDL code, or gate-level netlist, or an analogue function.

3.2.4 cell

specific circuit function including digital or analogue basic blocks

3.2.5 cell library

collection of all mutually compatible cells which conforms to a set of common constraints and standardized interfaces designed and characterized for a specified technology

3.2.6 code

string of words, numbers, letters and symbols that is used to model a DEVICE or its verification and validation environment

NOTE For example, Hardware Description Languages like VHDL, Verilog or SystemC are used to code DEVICE behavioral or synthesisable models, and code in other languages like C, Python or Tool Command Languages (Tcl) can be used in the DEVICE verification and validation.

3.2.7 data sheet

detailed functional, operational and parametric description of a DEVICE

NOTE A data sheet can include, for instance, a block diagram, truth table, pin and signal description, environmental, electrical and performance parameters, tolerances, timing information, and package description.

3.2.8 design for test

technique used to allow a complex integrated circuit to be tested with respect to potential manufacturing faults or to accelerate otherwise too slow validation tests

NOTE 1 For example, any dedicated circuits aimed to provide better observability or commandability of internal nodes of the DEVICE not accessible through primary inputs and outputs.

NOTE 2 Other examples of DFT are test busses, boundary scan as in JTAG, see IEEE 1149.1-2013, built-in self-test, and test modes for functional tests performed at DEVICE Validation, Qualification and Acceptance Phase.

3.2.9 design iteration

design changes that occur in any single phase or between two consecutive phases as defined in the DEVICE Development Plan, before the final DEVICE is released

3.2.10 DEVICE

integrated circuit or an IP Core

NOTE 1 A DEVICE can be a digital, analogue or mixed-signal ASIC, a programmed FPGA, a blank FPGA, a microprocessor, and a model of an IC function that is conceived for reuse as an IP Core.

NOTE 2 A DEVICE can also be a group of dice or chiplets interconnected and integrated inside a single package, such as a system-in-package or a multi-chip-module.

3.2.11 DEVICE Database

set of all digital files that are needed for the development of a DEVICE

NOTE 1 Examples of files integrating this database are behavioral and HDL models of the DEVICE, layout description files, models of the DEVICE system environment used to verify by simulation the DEVICE functionality, configuration files and SW programs used for the automation of the verification and validation of the DEVICE, input and output files used and generated by the different CAD tools used, for example files describing the resources, area, timing and power constraints, stimuli and expected output values files, or FPGA bit stream binary files.

NOTE 2 This database of files is incrementally updated throughout the DEVICE development phases, and all necessary elements that enable support, maintenance and a new development of the same or a modified version of the DEVICE can be found in the DEVICE database at the end of the DEVICE Validation, Qualification and Acceptance Phase.

3.2.12 DEVICE development flow

selection and sequence of engineering methods and tools applied during the definition, design, verification, implementation and validation of the DEVICE

3.2.13 DEVICE model

textual or graphical representation of a DEVICE, or a part of it, which defines one or several DEVICE characteristics

NOTE 1 For example, digital or analogue functional behavior, timing performance, power