SLOVENSKI STANDARD
SIST EN IEC 60749-28:2022

01-junij-2022

Nadomešča:
SIST EN 60749-28:2017

Polprevodniški elementi - Metode za mehansko in klimatsko preskušanje - 28. del: Preskušanje občutljivosti na elektrostatično razelektritev (ESD) - Model z elektrostatično nabitim elementom (CDM) - Raven elementa (IEC 60749-28:2022)

Semiconductor devices - Mechanical and climatic test methods - Part 28: Electrostatic discharge (ESD) sensitivity testing - Charged device model (CDM) - Device level (IEC 60749-28:2022)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 28: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Charged Device Model (CDM) - Device Level (IEC 60749-28:2022)

Dispositifs à semiconducteurs - Méthodes d'essai mécaniques et climatiques - Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle de dispositif chargé par contact direct (DC-CDM) (IEC 60749-28:2022)

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EN IEC 60749-28

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English Version

Semiconductor devices - Mechanical and climatic test methods - Part 28: Electrostatic discharge (ESD) sensitivity testing - Charged device model (CDM) - device level (IEC 60749-28:2022)

Dispositifs à semiconducteurs - Méthodes d'essai mécaniques et climatiques - Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle de dispositif chargé (CDM) - niveau du dispositif (IEC 60749-28:2022)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 28: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Charged Device Model (CDM) - Device Level (IEC 60749-28:2022)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

European foreword

The text of document 47/2746/FDIS, future edition 2 of IEC 60749-28, prepared by IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 60749-28:2022.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2023-01-05
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2025-04-05

This document supersedes EN 60749-28:2017 and all of its amendments and corrigenda (if any).

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Endorsement notice

The text of the International Standard IEC 60749-28:2022 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following note has to be added for the standard indicated:

IEC 60749-26 NOTE Harmonized as EN IEC 60749-26

IEC 60749-28

Edition 2.0 2022-03

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

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Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de dispositif chargé (CDM) – niveau du dispositif

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

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IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices, in collaboration with IEC technical committee 101: Electrostatics. It is an International Standard.

ANSI/ESDA/JEDEC JS-002-2018 has served as a basis for the elaboration of this standard. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association. ANSI/ESDA/JEDEC JS-002-2018 describes the field-induced (FI) method. An alternative, the direct contact (DC) method (not based on JS-002-2018), is described in Annex J.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) a new subclause and annex relating to the problems associated with CDM testing of integrated circuits and discrete semiconductors in very small packages;

b) changes to clarify cleaning of devices and testers.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2746/FDIS	47/2754/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex J.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
CDM ESD
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

3.2
CDM ESD tester
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

3.3
C_{Small}
device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below which it has been determined that CDM testing is not required if specified conditions are met

3.4
dielectric layer
thin insulator placed atop the field plate used to separate the device from the field plate

3.5
field plate
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

3.6
ground plane
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

3.7
software voltage
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

3.8
test condition
TC
tester plate voltage that meets the waveform parameter conditions

Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

4 Required equipment

4.1 CDM ESD tester

4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

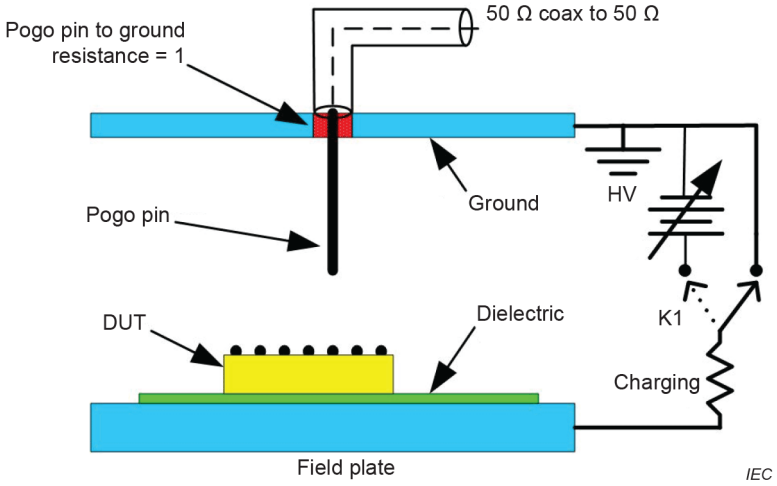

Figure 1 – Simplified CDM tester hardware schematic

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.

4.1.2 Current-sensing element

A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.

The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.