SLOVENSKI STANDARD
oSIST prEN IEC 61189-2-808:2023

01-april-2023

Preskusne metode za električne materiale, tiskana vezja in druge povezovalne strukture in sestave - 2-808. del: Meritev toplotne upornosti sestava z metodo toplotnega prehajanja

Test methods for electrical materials, printed board and other interconnection structures and assemblies - Part 2-808: Thermal resistance of an assembly by thermal transient method

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SECRETARIAT: Japan	SECRETARY: Mr Masahide Okamoto
OF INTEREST TO THE FOLLOWING COMMITTEES:	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.
FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY	
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TITLE:

Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-808: Thermal resistance of an assembly by thermal transient method

PROPOSED STABILITY DATE: 2028

NOTE FROM TC/SC OFFICERS:

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-808: Thermal resistance of an assembly by thermal transient method

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
XX/XX/FDIS	XX/XX/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

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92 • reconfirmed,
93 • withdrawn,
94 • replaced by a revised edition, or
95 • amended.
96

97 The National Committees are requested to note that for this document the stability date
98 is 2028..

99 THIS TEXT IS INCLUDED FOR THE INFORMATION OF THE NATIONAL COMMITTEES AND WILL BE DELETED
100 AT THE PUBLICATION STAGE.

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Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-808: Thermal resistance of an assembly by thermal transient method

1 Scope

This document describes the thermal transient method to characterize the thermal resistance of an assembly consisting of a heat source (e.g. power device), an attachment material (e.g. solder) and a dielectric layer with electrode. It is suitable to determine the thermal resistance of materials and assembly methods as well as to optimize the thermal flux to a heat sink.

Note: This method is not intended to measure and specify the value of the thermal resistance of a dielectric material. For that purpose, other standards exist. Examples are given in Annex A.

2 Normative references

JESD51-14 Transient Dual Interface Test Method

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

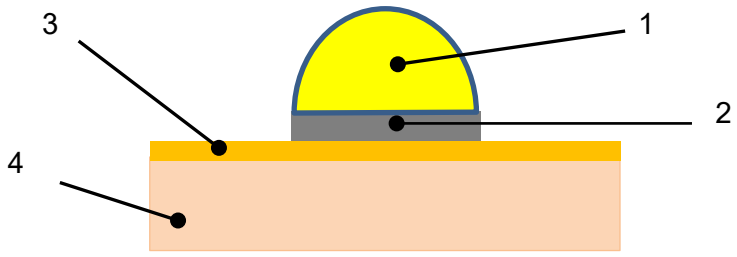
- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 Objective

The increasing power consumption of devices such as LED require a close examination of the heat dissipating path within thermal conductive printed circuit boards. Therefore, effective removal of heat to maintain a safe junction temperature is the key to meet the heat flux by using thermal conductive material for printed circuit boards. Thermal resistance is the crucial factor of heat dissipation dielectric materials in printed circuit board. Therefore, with the aim to reduce the thermal resistance in circuit boards, it is proposed to determine the thermal resistance by measuring the thermal transient characteristics of an assembly.

5 Test specimen

To test the thermal resistance of an assembly, at first a test specimen shall be built, which consists of a heat source (e.g. power device), an attachment material (e.g. solder) and a dielectric layer with metal electrode. See Figure 1 for the structure. In the next step, the thermal resistance of the assembly can be determined by comparison of the thermal transient characteristics obtained when testing the assembly attached to a thermostat with or without a thermal interface material (TIM). See Figure 3 and Clause 6 for the test description.



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1	Power source
2	Solder
3	Electrode layer
4	Dielectric layer

149 **Figure 1 – Structure of an assembly**

150 To obtain an adequate thermal resistance a layer of around 200 µm thick solder shall be used
151 for die attach. The power source is a chip type device of the size 3,45 mm x 3,45 mm, powered
152 with 1 W through VCC and GND. The dielectric layer is a 2 cm x 2 cm substrate of 1 mm
153 thickness. Figure 2 shows the example of such a test specimen.

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1	VCC
2	GND

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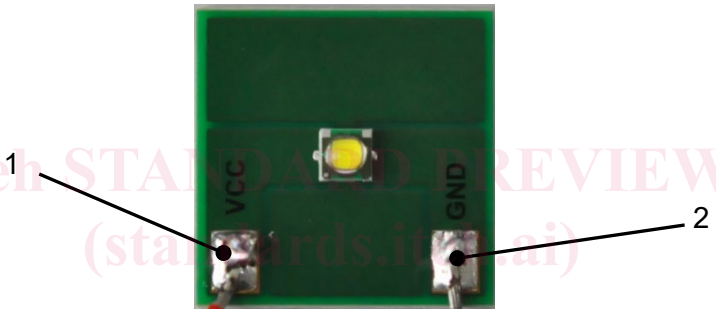

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157 **Figure 2 – The fabricated test sample**

158 ## 6 Test equipment and procedures

159 6-1 Test method and recommended test parameters

160 The thermal transient test equipment is a unique equipment for performing thermal
161 measurements on semiconductor devices like ICs, transistors, diodes etc. The thermal transient
162 test equipment is most suitable for analyzing their thermal behavior, evaluating packages and
163 device mounting, and detecting defects. This equipment is a computer-controlled equipment
164 that can be used along with a PC hosting a special control and evaluation software. This
165 equipment as a mandatory part of configuration can apply programmed thermal excitations and
166 record complex thermal responses and provides built-in results evaluation procedures. Results
167 of these post-processing procedures include the pulse thermal resistance diagram, time-
168 constant spectrum, complex locus of the thermal impedance, differential and integral structure
169 or profile function.

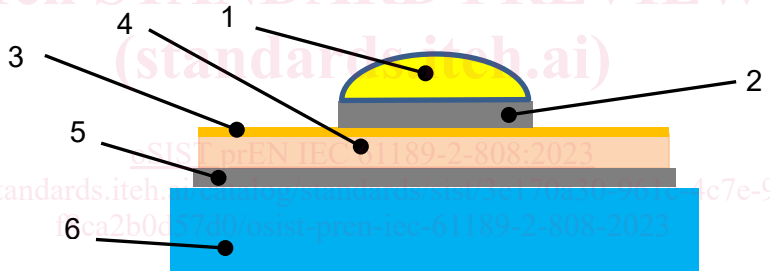
170 6-2 Test equipment

171 The thermal transient measurements can be performed using a commercially available test
172 equipment T3ster®[1] and specifically built test fixtures. Test sample is mounted on the
173 temperature-controlled heat sink. The heat sink is maintained at a temperature of 25°C and
174 controlled by a Keithley temperature controller. Initially, a junction-to-case thermal equilibrium
175 is ensured by applying a drive current (Idrive) for a sufficiently long duration; then the Idrive is
176 switched off and a small sense current (Isense) is applied. When the system shifts to its new
177 thermal equilibrium, the cooling down of the junction is measured.

178 1 T3ster® equipment is the trademark of a product supplied by MICRED (now Mentor Graphics).
179 This information is given for the convenience of users of this document and does not constitute

an endorsement by IEC of the product named. Equivalent products may be used if they can be shown to lead to the same results.

From the transient time curves, the duration of cooling down can be taken for how long the heating current Idrive needs to be applied to load the thermal capacities. The same time must be measured applying Isense to resolve the thermal path downstream to the respective capacity. One approach to determine the required measurement time is to modify the thermal interface between the heat sink and the module. The time value at which the curve with the best possible thermal interface and one with bad thermal interface separate is approximately the appropriate time duration for Idrive and Isense when the thermal path upstream the varied thermal interface is to be investigated. One can stepwise shorten the heat-up and cool down time afterward and observe at what setting, and at which time, values change in the logarithmic time-derived curve. The shortest time for which the deviation of the time curves is still within the signal-to-noise range of the curve with long heating and cooling times is still acceptable. The thermal response at initial '0' cycles and after 'n' cycles was measured. The measurement time of 40s is unnecessarily long. For the second test run with test samples B the measurement time was reduced to 5s. In principle, this allowed us to reduce the heating up and cooling down time further to 0.5s, because data later than 300ms are not included for data analysis. The shape of the transient signal does not change when cycle of heating up and cooling down times is shortened. In this experimental, the thermal tape (Thermal conductivity: 6.5 W/mK) with the thickness of 500 μm is used. Thermal tape as thermal interface material is used for separating the interface of the test sample through the comparison of thermal transient characteristics depending on with or without thermal interface material.



1	Power source (1W)
2	SAC305 solder (T: 200um)
3	Electrode layer (T: 35um)
4	Dielectric layer (T: 500um)
5	Thermal interface material (T: 500um)
6	Thermostat

Figure 3 – Test structure for measuring thermal resistance

- Noted: Thermostat is the temperature-controlled system (Annex D). Thermostat has the thermocouples inside system.

6-3 Test procedure

The test sequences to test the thermal resistance of an assembly are as follows.

1) Cleaning the contamination on the thermostat.

2) Firstly, attaching the test sample on the thermostat without the thermal interface material.

3) Testing the thermal transient characteristics of the test sample by biasing the power.

- Driving Current (Idrive): 1500 mA
- Sensor Current (Isense) for Test: 10 mA
- Total Power: 4.548 W
- TIM: Thermal pad (Thickness: 500um)
- Temperature Coeff.: -1.272 mV/℃

4) Repeat the sequence 1).

5) Secondly, attaching the test sample on the thermostat by using thermal interface material.

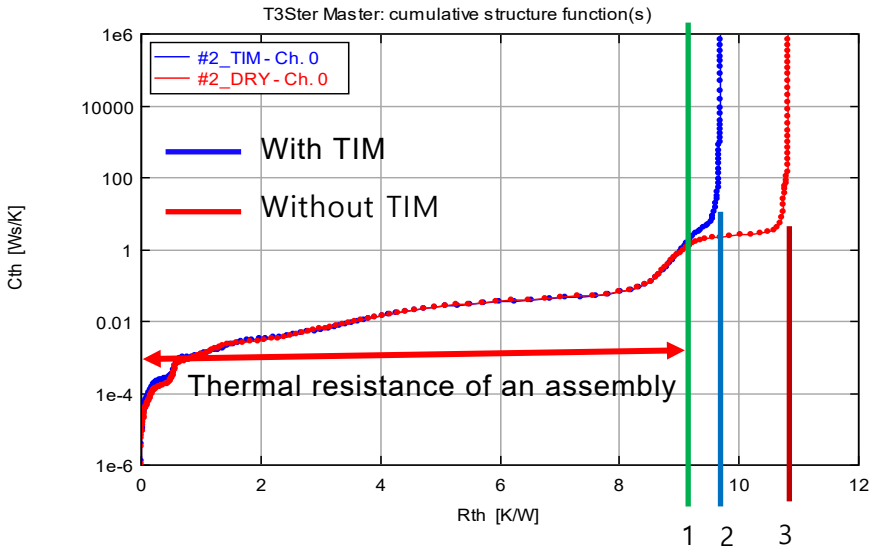
6) Testing the thermal transient characteristics of the test sample by biasing the power.

7) Comparing the thermal transient characteristics of the test sample depending on with or without the thermal interface material.

8) Extracting the thermal resistance value of an assembly with test results.

7 Test result

From the cumulative structure function of the thermal transient characteristics after converting to the cumulative structure function because it is eased to look for the separation point, the thermal resistance value is extracted by looking for the separated point from the measurement excel sheet instead of the visible graph (see Figure 4 and Table 1). It needs to refer to the standards of JESD-51-14 clause 4 Junction-to-Case Thermal Resistance Measurement (Test Method) for the detailed information.



1	The measured of thermal resistance of an assembly
2	The measured thermal resistance of assembly without TIM
3	The measured thermal resistance of assembly with TIM

Figure 4 – Test result for thermal resistance of an assembly

Note: Cth is thermal capacitance and K is temperature (Kelvin).

Note: In order to extract value for thermal resistance of assembly, it should look for the separated value from the measurement results depending on with TIM and without TIM.

Table 1 – Test result for thermal resistance of an assembly

Total thermal resistance (without TIM), K/W	Total thermal resistance (with TIM), K/W	Thermal resistance of an assembly, K/W
10.86	9.68	9.2

8 Report

This test method shall include:

a) structure of test specimen

b) thermal tape used as TIM.

c) the used power sources.

d) the date of the test.

e) the room temperature under which the test was conducted.

f) the test sequences.

g) the graph of the cumulative structure function

h) the total thermal resistance of test specimen with or without TIM.

i) the thermal resistance of an assembly

Noted: The result value of an assembly separated differently from the measurement results depending on the presence or absence of TIM is defined as the thermal resistance of and assembly. It shall refer to JESD-51-14 clause 4 Junction-to-Case Thermal Resistance Measurement (Test Method).

9 Bibliographies

JESD51-14 Transient Dual Interface Test Method

JESD-51-50: Overview of Methodologies for the Thermal Measurement of Single- and Multi-Chip, Single- and Multi-PN-Junction Light-Emitting Diodes (LEDs)

JESD-51-51: Implementation of the Electrical Test Method for the Measurement of the Real Thermal Resistance and Impedance of Light-emitting Diodes with Exposed Cooling Surface

JEDEC Solid State Technology Association (JEDEC Standard)

JEDEC JESD51-1: INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):