

# SLOVENSKI STANDARD oSIST prEN IEC 61188-6-3:2023

01-oktober-2023

## Plošče tiskanih vezij in sestavi plošč tiskanih vezij - Zasnova in uporaba - 6-3. del: Razmestitev priključkov - Opis razmestitve priključkov skozi luknje komponent

Circuit boards and circuit board assemblies - Design and use - Part 6-3: Land pattern design - Description of land pattern for through hole components (THT)

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# DSIST prEN IEC 61188-6-3:2023

Ta slovenski standard je istoveten z: prEN IEC 61188-6-3:2023

## <u>ICS:</u>

31.180 Tiskana vezja (TIV) in tiskane Printed circuits and boards plošče
31.190 Sestavljeni elektronski elementi Electronic component assemblies

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en

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# 91/1878/CDV

#### COMMITTEE DRAFT FOR VOTE (CDV)

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IEC TC 91 : ELECTRONICS ASSEMBLY TECHNOLOGY			
SECRETARIAT:	SECRETARY:		
Japan	Mr Osamu IKEDA		
OF INTEREST TO THE FOLLOWING COMMITTEES:	PROPOSED HORIZONTAL STANDARD:		
	Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.		
FUNCTIONS CONCERNED:			
	QUALITY ASSURANCE		
SUBMITTED FOR CENELEC PARALLEL VOTING	NOT SUBMITTED FOR CENELEC PARALLEL VOTING		
Attention IEC-CENELEC parallel voting			
The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting.	<u>61188-6-3:2023</u> ards/sist/3cdadde7-f9a8-492c-b2f1-		

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TITLE:

Circuit boards and circuit board assemblies - Design and use - Part 6-3: Land pattern design - Description of land pattern for through hole components (THT)

PROPOSED STABILITY DATE: 2025

NOTE FROM TC/SC OFFICERS:

The revised CDV draft was approved.at the TC91 WG12 meeting in June 2023.

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	ΙE	C CDV 61188-6-3 © IEC 2023 4 91/1878/CDV		
60		INTERNATIONAL ELECTROTECHNICAL COMMISSION		
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63		CIRCUIT BOARDS AND CIRCUIT BOARD ASSEMBLIES		
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65		- DESIGN AND USE -		
66 67		Part 6-3: I and nattern design - Description of land nattern for through hole		
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71		FOREWORD		
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107 The text of this International Standard is based on the following documents:

FDIS	Report on voting
XX/XX/FDIS	XX/XX/RVD

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Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

111 This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- 115 reconfirmed,
- 116 withdrawn,
- 117 replaced by a revised edition, or
- 118 amended.
- 119

The National Committees are requested to note that for this document the stability date is 20XX.. THIS TEXT IS INCLUDED FOR THE INFORMATION OF THE NATIONAL COMMITTEES AND WILL BE DELETED AT THE PUBLICATION STAGE.

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#### INTRODUCTION

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126 The new series IEC 6188-6-xx replaces the below listed documents:

127 IEC 61188-5-1 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-1: 128 Attachment (land/joint) considerations - Generic requirements

IEC 61188-5-2 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-2:
 Attachment (land/joint) considerations - Discrete components

IEC 61188-5-3 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-3:
 Attachment (land/joint) considerations - Components with gull-wing leads on two sides

IEC 61188-5-4 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-4:
 Attachment (land/joint) considerations - Components with J leads on two sides

IEC 61188-5-5 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-5:
 Attachment (land/joint) considerations - Components with gull-wing leads on four sides

IEC 61188-5-6 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-6:
 Attachment (land/joint) considerations - Chip carriers with J-leads on four sides

IEC 61188-5-8 Ed. 1.0 Printed boards and printed board assemblies - Design and use - Part 5-8:
 Attachment (land/joint) considerations - Area array components (BGA, FBGA, CGA, LGA)

141 The content of above documents is based on IPC-782 Rev. A with Amendment 1 & 2, which was replaced

in 2002 by IPC-7351. The component spectrum and pitch levels have dramatically changed since publication of the 61188-5-xx series and its dimensioning concept does not longer fulfil state of the art

144 mounting and soldering requirements.

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#### CIRCUIT BOARDS AND CIRCUIT BOARD ASSEMBLIES 146 147 - DESIGN AND USE -148 149 Part 6-3: Land pattern design - Description of land pattern for through hole 150 components (THT) 151 152 153 154 Scope 155 1 This International Standard specifies the requirements for lands and land pattern on circuit boards for 156 the mounting of components with leads by soldering based on the solder joint requirements of the IEC 157 61191-1, and IEC 61191-3. 158 159 Normative references 2 160 The following documents are referred to in the text in such a way that some or all of their content 161 constitutes requirements of this document. For dated references, only the edition cited applies. For 162 undated references, the latest edition of the referenced document (including any amendments) applies. 163

164 IEC 61191-1, Printed board assemblies – Part 1: Generic specification – Requirements for soldered 165 electrical and electronic assemblies using surface mount and related assembly technologies

IEC 61191-3, *Printed board assemblies – Part 3: Sectional specification –* Requirements for through hole mount soldered assemblies

168 IEC 60194, Printed board design, manufacture and assembly – Terms and definitions

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843169367660/osist-pren-iec-61188-6-3-2023

# **3 Terms and definitions**

For the purposes of this document, the terms and definitions given in IEC 60194-2, and the following apply.

173 ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at <u>http://www.iso.org/obp</u>
- 176

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# 177 3.1 Annular ring

178 It is defined as the amount of land that remains after a hole is drilled in the defined padstack

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#### 180 **3.2 Finished hole size (FSH)**

The diameter after all metallization processes (galvanic processing) and additional surface
 finishing processes (final finish)

#### 184 **3.3 Solder source side**

The side which is in contact with solder material (e.g. soldering wave, solder tip), It is usually
 the opposite side of the assembled THT component

#### 188 3.4 Solder target side

The side where the component is usually placed. The solder material will fill the THT from the opposite side (solder source side)

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#### **4 Description of a through hole Component**

#### 194 4.1 Component body

Leaded components consist of a so called body with electrical functional elements and leads which
 enable the connection to the circuitry of the circuit board by soldering (see Figure 1).



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#### Figure 1 – Leaded component

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#### 201 4.2 Component leads

Leads of components for through hole mounting usually have a round, square or rectangular profile. For the padstack design the maximum diameter of the lead is the determining parameter. The diameter of the through hole depends on the shape of the lead (Typical variations of leads see Figure 2, Figure 3 and Figure 4).

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A **Padstack** is the **definition** of the size and shape of the **pads** on each of the layers of a circuit board plus the definition of the hole size and type. Form and size of the pad depends on the lead form and size and the component body.

#### 219 5.2 Pad types

Depending on the layer function in the circuit board layer stack the pad function also will be different. Table 1 gives an overview about the relation between layer functionality and associated pad type.

222

#### Table 1 – Layer function and pad types

Layer function	Pad type	display
Solder mask	Top and Bottom Solder Mask	negative data
Outer layer	Top and Bottom Pad (Land)	positive data
Inner signal layer	Inner Layer Pad	positive data
Inner power layer	Plane Thermal or Plane Anti-Pad	negative data

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Figure 5 – Padstack

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#### 227 5.2.1 Solder mask pads

The solder mask pads define the metallic surface of the solder joint. Within the CAD tool the solder mask is displayed inverse

#### 230 5.2.2 Outer layer pads



Outer layer pads describe the copper area which fixe the soldered device with the outer layer. Sometimes it can be helpful to distinguish between the component and the solder side.

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# 233 **5.2.3 Thermal pads** 843169367660/osist-pren-iec-61188-6-3-20

The feature of a thermal pad is used to prohibit heat dissipation during the soldering process to get a reliable solder joint without degrading the circuit board base material.

#### 236 5.2.4 Anti pads

The so called anti pad are used to ensure insulation between the inner layer copper pads and the copper area of power planes. Usually the minimum size of the anti-pad is the minimum isolation distance of copper elements with different nets and the size of the inner layer pad.

#### 240 5.3 Pad shapes

The basic elements of the Padstacks are polygons on each layer which represent the copper structures of the circuit board. These polygons can be circular, square or rectangular with rounded or chamfered corners or even variations of this shapes.

Sometimes a special pad shape like a square pad on the component layer of the circuit board is used as pin 1 indicator.

#### 246 **5.4 Holes**

#### **5.4.1 Considerations for plated through hole dimensioning**

The used assembly technique has a influences on the hole diameter, additionally the number of pins per device and their alignment. Different assembly techniques shall have different hole calculations:

• The way of creating the hole (drilling, milling, punching, additive manufacturing, others)