SLOVENSKI STANDARD
SIST EN IEC 63373:2022

01-maj-2022

Smernice za dinamične metode preskusov odpornosti za naprave za pretvorbo energije na osnovi GaN HEMT (IEC 63373:2022)

Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices (IEC 63373:2022)

Richtlinien für Prüfverfahren des dynamischen Einschaltwiderstandes bei GaN-HEMT-Leistungswandlern (IEC 63373:2022)

Lignes directrices pour les méthodes d’essai de résistance dynamique à l’état passant des dispositifs de conversion de puissance fondés sur les HEMT en GaN (IEC 63373:2022)

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

Ta slovenski standard je istoveten z: EN IEC 63373:2022

ICS:

31.080.99	Drugi polprevodniški elementi	Other semiconductor devices

SIST EN IEC 63373:2022 en

2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

SIST EN IEC 63373:2022

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

SIST EN IEC 63373:2022

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN IEC 63373

March 2022

ICS 31.080.99

English Version

Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices (IEC 63373:2022)

Lignes directrices pour les méthodes d'essai de résistance dynamique à l'état passant des dispositifs de conversion de puissance fondés sur les HEMT en GaN (IEC 63373:2022)

Richtlinien für Prüfverfahren des dynamischen Einschaltwiderstandes bei GaN-HEMT-Leistungswandlern (IEC 63373:2022)

This European Standard was approved by CENELEC on 2022-03-17. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

iTeh STANDARD PREVIEW (standards.iteh.ai)

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Republic of North Macedonia, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

© 2022 CENELEC All rights of exploitation in any form and by any means reserved worldwide for CENELEC Members.

Ref. No. EN IEC 63373:2022 E

SIST EN IEC 63373:2022

European foreword

The text of document 47/2690/CDV, future edition 1 of IEC 63373, prepared by IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 63373:2022.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2022-12-17
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2025-03-17

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

Any feedback and questions on this document should be directed to the users' national committee. A complete listing of these bodies can be found on the CENELEC website.

iTeh STANDARD PREVIEW (standards.iteh.ai)

Endorsement notice

The text of the International Standard IEC 63373:2022 was approved by CENELEC as a European Standard without any modification.

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

SIST EN IEC 63373:2022

IEC 63373

Edition 1.0 2022-02

INTERNATIONAL STANDARD

NORME INTERNATIONALE

iTeh STANDARD PREVIEW
(standards.iteh.ai)

Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices

Lignes directrices pour les méthodes d'essai de résistance dynamique à l'état passant des dispositifs de conversion de puissance fondés sur les HEMT en GaN

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.080.99 ISBN 978-2-8322-1076-6

Warning! Make sure that you obtained this publication from an authorized distributor.
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

® Registered trademark of the International Electrotechnical Commission
Marque déposée de la Commission Electrotechnique Internationale

SIST EN IEC 63373:2022

CONTENTS

FOREWORD ... 3
INTRODUCTION ... 5
1 Scope ... 6
2 Normative references ... 6
3 Terms, definitions, symbols and abbreviated terms ... 6
3.1 Terms and definitions ... 6
3.2 Symbols and abbreviated terms ... 6
4 Test circuits and waveforms ... 7
4.1 General ... 7
4.2 Inductive and resistive switching methods ... 7
4.3 Pulsed current-voltage (I-V) method ... 10
5 Requirements ... 12
Bibliography ... 14

Figure 1 – Inductive-resistive load "double-pulse" test circuit for hard-switching evaluation ... 8
Figure 2 – Depiction of the hard-switching "double-pulse" test circuit (showing its similarity to a boost converter) ... 8
Figure 3 – Simplified flowchart for inductive and/or resistive switching based dynamic on-resistance test ... 9
Figure 4 – Representative continuous-pulse hard-switching waveforms for measuring dynamic on-resistance using the test circuits in Figure 1 and Figure 2 ... 10
Figure 5 – Example test circuit for soft-switching on-resistance measurement (the gate and drain terminals are pulsed with independent voltage signals) ... 10
Figure 6 – Simplified flowchart for soft switching based dynamic on-resistance test ... 11
Figure 7 – Illustrative timing diagram for measuring dynamic ON-resistance under OFF-state stress in soft-switching mode ... 12

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

SIST EN IEC 63373:2022

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/bc5af23d-7f15-4b7f-9089-8479a3e3712a/sist-en-iec-63373-2022

IEC 63373 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

This standard is based upon JEP173 [1].[1] It is used with permission of the copyright holder, JEDEC Solid State Technology Association.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2690/CDV	47/2735/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

1 Numbers in square brackets refer to the Bibliography.

SIST EN IEC 63373:2022

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The "colour inside" logo on the cover page of this document indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

SIST EN IEC 63373:2022

INTRODUCTION

This document is intended for use in the GaN power semiconductor and related power electronic industries, and provides guidelines for measuring the dynamic ON-resistance of GaN power devices.

Gallium Nitride (GaN) lateral power High Electron Mobility Transistor (HEMT) conducts through a two-dimensional electron gas (2DEG) in ON-state operation. Due to the various stress conditions that the device encounters during power electronic switching applications, some charge could get trapped in specific regions of the transistor structure. The trapped electrons cause an increased ON-resistance when operated in a switching environment. This phenomenon is known as current collapse and the ON-resistance at switching operation is called dynamic ON-resistance in order to distinguish from DC ON-resistance. Increased dynamic ON-resistance translates to higher power loss, thereby reducing overall system efficiency. Not verifying the dynamic ON-resistance characteristic can put GaN device reliability at risk [2].

The test methods provided in this document can be used as a guideline for measuring dynamic ON-resistance of GaN power device, focused on lateral HEMT technologies. These three test methods can be applied for datasheet, process control, technology development, final tests and other usage. Parasitic effects impact high precision measurements and wafer level tests can minimize parasitic effects. Additionally, self-heating can impact the package level tests depending upon the package thermal characteristics.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

SIST EN IEC 63373:2022

DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES

1 Scope

In general, dynamic ON-resistance testing is a measure of charge trapping phenomena in GaN power transistors. This publication provides guidelines for testing dynamic ON-resistance of GaN lateral power transistor solutions. The test methods can be applied to the following:

a) GaN enhancement and depletion-mode discrete power devices [3];

b) GaN integrated power solutions;

c) the above in wafer and package levels.

The prescribed test methods can be used for device characterization, production testing, reliability evaluations and application assessments of GaN power conversion devices. This document is not intended to cover the underlying mechanisms of dynamic ON-resistance and its symbolic representation for product specifications.

2 Normative references

There are no normative references in this document.

3 Terms, definitions, symbols and abbreviated terms

iTeh STANDARD PREVIEW
(standards.iteh.ai)

3.1 Terms and definitions

SIST EN IEC 63373:2022
https://standards.iteh.ai/catalog/standards/sist/6c5af23d-7f15-4b7f-9080-8479a3e3712c/sist-en-iec-63373-2022

No terms and definitions are listed in this document.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.2 Symbols and abbreviated terms

Symbol or abbreviation	Name or term
DUT	Device Under Test
V_{DD}	Supply voltage
V_{DS}	Drain to Source Voltage of DUT
V_{GS}	Gate to Source Voltage of DUT
D1	Free-wheeling diode
L	Inductance
R	Resistance
C	Capacitance
I_D	Drain current of DUT in ON-state
$V_{DS(ON)}$	Drain to Source Voltage of DUT in ON-state
$R_{DS(ON)}$	Drain to Source Resistance of DUT in ON-state