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Standard Test Method for Measuring Dose Rate Threshold for Upset of Digital Integrated Circuits (Metric)¹

This standard is issued under the fixed designation F744M; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the measurement of the threshold level of radiation dose rate that causes upset in digital integrated circuits under static operating conditions. The radiation source is either a flash X-ray machine (FXR) or an electron linear accelerator (LINAC).

1.2 The precision of the measurement depends on the homogeneity of the radiation field and on the precision of the radiation dosimetry and the recording instrumentation.

1.3 The test may be destructive either for further tests or for purposes other than this test if the integrated circuit being tested absorbs a total radiation dose exceeding some predetermined level. Because this level depends both on the kind of integrated circuit and on the application, a specific value must be agreed upon by the parties to the test (6.8).

1.4 Setup, calibration, and test circuit evaluation procedures are included in this test method.

1.5 Procedures for lot qualification and sampling are not included in this test method.

1.6 Because of the variability of the response of different device types, the initial dose rate for any specific test is not given in this test method but must be agreed upon by the parties to the test.

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~~1.7 The values stated in SI units are to be regarded as standard. No other units of measurement are included in this standard.~~

~~1.8 This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.~~

2. Referenced Documents

2.1 *ASTM Standards:*²

E665 [Practice for Determining Absorbed Dose Versus Depth in Materials Exposed to the X-Ray Output of Flash X-Ray Machines](#)³

E666 [Practice for Calculating Absorbed Dose From Gamma or X Radiation](#)

E668 [Practice for Application of Thermoluminescence-Dosimetry \(TLD\) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices](#)

E1894 [Guide for Selecting Dosimetry Systems for Application in Pulsed X-Ray Sources](#)

F526 [Test Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests](#)

3. Terminology

~~3.1 Definitions of Terms Specific to This Standard:~~

~~3.1.1 *determined integrated circuit*—integrated circuit whose output is a unique function of the inputs; the output changes if and only if the input changes (for example, AND- and OR-gates).~~

~~3.1.2 *dose rate*—energy absorbed per unit time and per unit mass by a given material from the radiation to which it is exposed.~~

~~3.1.3 *dose rate threshold for upset*—minimum dose rate that causes either: (1) the instantaneous output voltage of an operating~~

¹ This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Nuclear and Space Radiation Effects.

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² For referenced ASTM standards, visit the ASTM website, www.astm.org, or contact ASTM Customer Service at service@astm.org. For *Annual Book of ASTM Standards* volume information, refer to the standard's Document Summary page on the ASTM website.

³ Withdrawn.

³ Withdrawn. The last approved version of this historical standard is referenced on www.astm.org.

digital integrated circuit to be greater than the specified maximum LOW value (for a LOW output level) or less than the specified minimum HIGH value (for a HIGH output level), or (2) a change of state of any stored data.

3.1.4 ~~nondetermined integrated circuit~~ non-determined integrated circuit—integrated circuit whose output or internal operating conditions are not unique functions of the inputs (for example, flip-flops, shift registers, and RAMs).

4. Summary of Test Method

4.1 The test device and suitable dosimeters are irradiated by either an FXR or a ~~LNAC~~ linac. The test device is operating but under static conditions. The output(s) of the test device and of the dosimeters are recorded.

4.2 The dose rate is varied to determine the rate which results in upset of the test device.

4.3 For the purposes of this test method, upset is considered to be either of the following:

4.3.1 An output voltage transient exceeding a predetermined value, or

4.3.2 For devices having output logic levels which are not unique functions of the input logic levels, such as flip-flops, a change in the logic state of an output.

4.3.3 For non-determined integrated circuits, a change of state of an internal storage element or node.

4.4 A number of factors are not defined in this test method, and must be agreed upon beforehand by the parties to the test:

4.4.1 Total ionizing dose limit (see 1.3),

4.4.2 Transient values defining an upset (see 4.3.1),

4.4.3 Temperature at which the test is to be performed (see 6.7),

4.4.4 Details of the test circuit, including output loading, power supply levels, and other operating conditions (see 7.4, 10.3, and 10.4),

4.4.5 Choice of radiation pulse source (see 7.7),

4.4.6 Radiation pulse width (see 7.7.2),

4.4.7 Sampling (see 8.1),

4.4.8 Need for total ionizing dose measurement (see 6.8, 7.6, and 10.1),

4.4.9 Desired precision of the upset threshold (see 10.8), and

4.4.10 Initial dose rate (see 1.6 and 10.5).

5. Significance and Use

5.1 Digital integrated circuits are specified to operate with their inputs and outputs in either a logical 1 or a logical 0 state. The occurrence of signals having voltage levels not meeting the specifications of either of these levels (an upset condition) may cause the generation and propagation of erroneous data in a digital system.

5.2 Knowledge of the radiation dose rate that causes upset in digital integrated circuits is essential for the design, production, and maintenance of electronic systems that are required to operate in the presence of pulsed radiation environments.

6. Interferences

6.1 *Air Ionization*—A spurious component of the signal measured during a test can result from conduction through air ionized by the radiation pulse. The source of such spurious contributions can be checked by measuring the signal while irradiating the test fixture in the absence of a test device. Air ionization contributions to the observed signal are generally proportional to the applied field, while those due to secondary emission effects (6.2) are not. The effects of air ionization external to the device may be minimized by coating exposed leads with a thick layer of paraffin, silicone rubber, or nonconductive enamel or by making the measurement in a vacuum.

6.2 *Secondary Emission*—Another spurious component of the measured signal can result from charge emission from, or charge injection into, the test device and test circuit.⁴ This may be minimized by shielding the surrounding circuitry and irradiating only the minimum area necessary to ensure irradiation of the test device. Reasonable estimates of the magnitude to be expected of current resulting from secondary-emission effects can be made based on the area of metallic target materials irradiated (see Note 1). Values generally range between 10^{-11} and 10^{-10} A·s/cm²·Gy, but the use of a scatter plate with an intense beam may increase this current (7.7.2).

NOTE 1—For dose rates in excess of 10^8 Gy(Si)/s, the photocurrents developed by the package may dominate the device photocurrent. Care should be taken in the interpretation of the measured photoresponse for these high dose rates.

6.3 *Orientation*—The effective dose to a semiconductor junction can be altered by changing the orientation of the test device with respect to the irradiating beam. Most integrated circuits may be considered “thin samples” (in terms of the range of the radiation). However, some devices may have cooling studs or thick-walled cases that can act to scatter the incident beam, thereby modifying the dose received by the semiconductor chip. Care must be taken in the positioning of such devices.

6.4 *Dose Enhancement*—High atomic number materials near the active regions of the integrated circuit (package, metallization, die attach materials, etc.) can cause an enhanced dose to be delivered to the sensitive regions of the device when it is irradiated

⁴ Sawyer, J. A., and van Lint, V. A. J., “Calculations of High-Energy Secondary Electron Emission,” *Journal of Applied Physics-Physics*, Vol 35, No. 6, June 1964, pp. 1706–1711.

with bremsstrahlung. Therefore, when an FXR is used as the radiation source, calculations should be performed to determine the possibility and extent of this effect.

6.5 *Electrical Noise*—Since radiation test facilities are inherent sources of r-f electrical noise, good noise-minimizing techniques such as single-point ground, filtered d-c supply lines, etc., must be used in these measurements.

6.6 *Temperature*—Device characteristics are dependent on junction temperature; hence, the temperature of the test should be controlled. Unless the parties to the test agree otherwise, measurements shall be made at room temperature ($23(24 \pm 5^\circ\text{C}), -6^\circ\text{C}$).

6.7 *Beam Homogeneity and Pulse-to-Pulse Repeatability*—The intensity of a beam from an FXR or a LINAC is likely to vary across its cross section. Since the pulse-shape monitor is placed at a different location than the device under test, the measured dose rate may be different from the dose rate to which the device was exposed. The spatial distribution and intensity of the beam may also vary from pulse to pulse. The beam homogeneity and pulse-to-pulse repeatability associated with a particular radiation source should be established by a thorough characterization of its beam prior to performing a measurement.

6.8 *Total Ionizing Dose*—Each pulse of the radiation source imparts an ionizing dose to both the device under test and the device used for dosimetry. The total ionizing dose deposited in a semiconductor device can change its operating characteristics. As a result, the response that is measured after several pulses may be different from that characteristic of an unirradiated device. Care should be exercised to ensure that the total ionizing dose delivered to the test device is less than the agreed-upon maximum value. Care must also be taken to ensure that the characteristics of the dosimeter have not changed due to the accumulated dose.

7. Apparatus

7.1 *Regulated d-c Power Supplies*—A power supply with floating outputs to produce the voltages required to bias the integrated circuit under test.

7.2 *Recording Devices*—A single dual-beam, or two single-beam oscilloscopes; equipped with cameras; or transient digitizers with transient digitizers, recording media, and appropriate displays. The bandwidth capabilities of the recording devices shall be such that the radiation responses of the integrated circuit and the pulse-shape monitor (7.6) are accurately displayed and recorded.

7.3 *Cabling*—To adequately complete the connection of the test circuit in the exposure area with the power supply and oscilloscopes in the data area. Shielded twisted pair or coaxial cables may be used to connect the power supplies to the bias points of the test circuit; however, coaxial cables properly terminated at the oscilloscope input are required for the signal leads.

7.4 *Test Circuit* (see Fig. 1)—Although the details of test circuits for this test must vary depending on the kind of integrated circuit to be tested and on the specific parameters of the circuit which are to be measured, Fig. 1 provides the information necessary for the design of a test circuit for most purposes. The capacitor, *C*, provides an instantaneous source of current as may be required by the integrated circuit during the radiation pulse. Its value must be large enough that the decrease in the supply voltage during a pulse is less than 10 %. The capacitor, *C*, should be paralleled by a small (approximately 0.01 μF) low-inductance capacitor to ensure that possible inductive effects of the large capacitor are offset. Both capacitors must be located as close to the integrated circuit socket as possible, consistent with the space needed for connection of the current transformer and for any shielding that may be necessary. The switch, *S*, provides means to place the output of the integrated circuit (here a NAND gate) in either a logic LOW or a logic HIGH state. The arrangement of the grounding connections provides that only one ground exists, at the point of

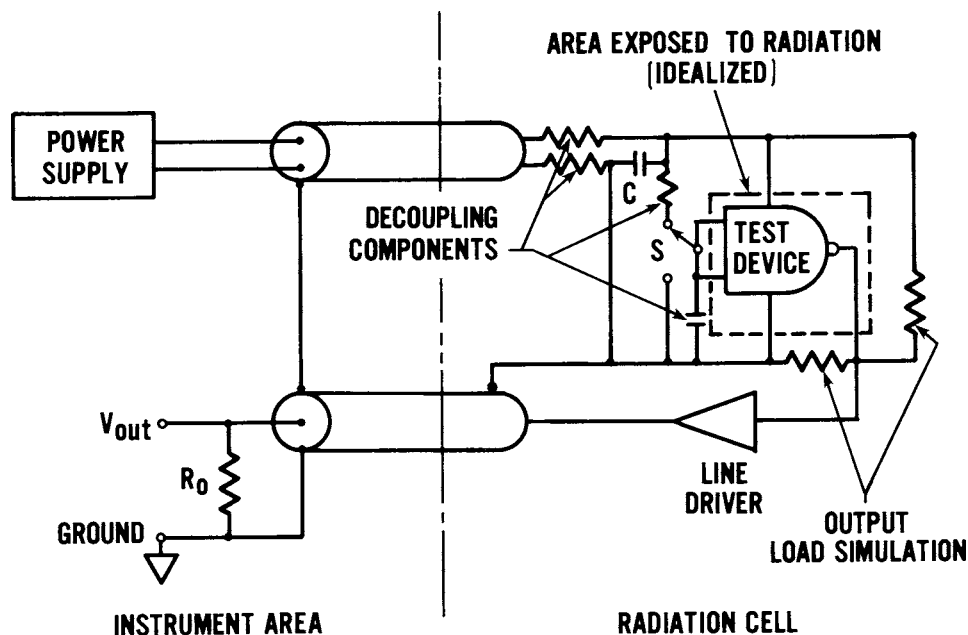


FIG. 1 Example of a Test Circuit—Example for a NAND Gate