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Space engineering - Guidelines for electrical design and interface requirements for power supply

Raumfahrttechnik - Richtlinien für die elektrische Konstruktion und Schnittstellenanforderungen für die Stromversorgung

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49.140	Vesoljski sistemi in operacije	Space systems and operations

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Space engineering - Guidelines for electrical design and interface requirements for power supply

Raumfahrttechnik - Richtlinien für die elektrische Konstruktion und Schnittstellenanforderungen für die Stromversorgung

This draft Technical Report is submitted to CEN members for Vote. It has been drawn up by the Technical Committee CEN/CLC/JTC 5.

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European Foreword

This document (FprCEN/TR 17603-20-20:2021) has been prepared by Technical Committee CEN/CLC/JTC 5 “Space”, the secretariat of which is held by DIN.

It is highlighted that this technical report does not contain any requirement but only collection of data or descriptions and guidelines about how to organize and perform the work in support of 16603-20.

This Technical report (FprCEN/TR 17603-20-20:2021) originates from ECSS-Q-HB-20-20A.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any TR covering the same scope but with a wider domain of applicability (e.g.: aerospace).

This document is currently submitted to the CEN CONSULTATION.

Introduction

The power distribution by Latching Current Limiters, or LCLs, has been widely used in almost all European satellites for some decades as an effective way to achieve a very controlled and reliable load connection and disconnection from the satellite main bus, including power management in case of overload and load short circuit failures.

Additionally, power distribution by LCLs minimises inrush current events due to load filters charging (see section 5.7.2.3), and for this reason effectively allows the reduction of the loads filters themselves.

On the other side power distribution by LCLs has always been matter of “local” discussion and review, while no attempt has been done so far to collect all the available information in a congruent and explanatory handbook and to allow a product-oriented specification as presently done with ECSS-E-ST-20-20.

This handbook complements ECSS-E-ST-20-20, and it is directed at the same time to power system engineers, who are specifying and procuring units containing LCLs for power distribution and protection, and to power electronics design engineers, who are in charge of designing and verifying power distribution by LCLs.

For the system engineers, this document explains the detailed issues at circuit level and the impacts of the requirements for the design of LCLs.

For design engineers, this document gives insight and understanding on the rationales of the requirements on their designs.

It is important to notice that the best understanding of the topic of Power Distribution based by LCLs is achieved by the contextual reading of both the present handbook and the ECSS-E-ST-20-20.

Note that the present issue of the handbook covers electrical design and interface requirements for power distribution based on Latching Current Limiters only.

Future issues of the present handbook will cover additional power interfaces.

1 Scope

In general terms, the scope of the consolidation of LCLs power distribution interface requirements in the ECSS-E-ST-20-20 and the relevant explanation in the present handbook is to allow a more recurrent approach for the specific designs offered by power unit manufacturers, at the benefit of the system integrators and of the Agency, thus ensuring:

- better quality,
- stability of performances, and
- independence of the products from specific mission targets.

A recurrent approach enables power distribution manufacturing companies to concentrate on products and a small step improvement approach that is the basis of a high quality industrial output.

In particular, the scope of the present handbook is:

- to explain the principles of operation of power distribution based on LCLs,
- to identify important issues related to LCLs, and
- to give some explanations of the requirements set up in the ECSS-E-ST-20-20 for power distribution based on LCLs, for both source and load sides.

2 References

EN Reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system - Glossary of terms
EN 17603-20-20	ECSS-E-ST-20-20	Space engineering - Electrical design and interface requirements for power supply
EN 16602-30-02	ECSS-Q-ST-30-02	Space product assurance - Failure modes, effects (and criticality) analysis (FMEA/FMECA)
EN 16602-30-11	ECSS-Q-ST-30-11	Space product assurance - Space product assurance, Derating – EEE components
	ESA PSS-02-10 Vol.1 Issue 1, Nov. 1992	Power standard
	IEEE CFP13APE-USB (2013)	MOSFET Gate Open Failure Analysis in Power Electronics, IEEE Applied Power Electronics Conference and Exposition, Long Beach, California, 17-21 March 2013, pp. 189-196 (reported as Annex G in the present HB)
	ESA SP-719 (2014)	Approach to design for stability a system comprising a non-ideal current source and a generic load, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex H in the present HB)
	ESA SP-719 (2014)	LCL current control loop stability design, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex I in the present HB)

3
Terms, definitions and abbreviated terms

3.1 Terms from other documents

a. For the purpose of this document, the terms and definitions from ECSS-S-ST-00-01 apply, in particular for the following terms:

1. **redundancy**
2. **active redundancy**
3. **hot redundancy**
4. **cold redundancy**
5. **fault**
6. **fault tolerance**

b. For the purpose of this document, the terms and definitions from ECSS-E-ST-20-20 apply.

3.2 Abbreviated terms

For the purpose of this document, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
A	analysis
BJT	bipolar junction transistor
EOL	end-of-life
ESTEC	European Space Technology and Research Centre
I	inspection
LCL	latching current limiter
MFET	MOS field effect transistor
MOS	metal oxide semiconductor
OVP	overvoltage protection
PCDU	power conditioning and distribution unit
PDU	power distribution unit
RDSON	drain source resistance in on state (for MFET)
RLCL	retriggerable LCL

Abbreviation	Meaning
RoD	review of design
S3R	sequential unit switching regulator
SOA	safe operating area
SPFF	single point failure free
T	test
TWTA	travelling wave tube amplifier
UVP	undervoltage protection
WCA	worst case analysis

4 Explanations

4.1 Explanatory note

The present handbook refers to the electrical interface requirements defined in the ECSS-E-ST-20-20.

The ECSS-E-ST-20-20 requirements are referred to in this handbook by using following convention and are indicated in *italic font*:

[requirement number] feature - sub-feature.

For example:

Requirement 5.2.3.2.1a.

Clause Heading 3 title = "Current Limitation Section"

Clause Heading 4 title = "Switch element, positions"

→ *[5.2.3.2.1.a.] Current Limitation Section – Switch element, position*

See also, for more information, Annex A of ECSS-E-ST-20-20.

In addition:

- each requirement (i.e. any statement containing a "shall" in the standard) is marked with **red text**.
- each recommendation (i.e. any statement containing a "should" in the standard) is marked with **blue text**.

Keywords are highlighted in **bold**. A keyword is a word that either has a special meaning in the contest of the chapter in which it appears, or highlight a concept.

4.2 How to use this document

For the best utilisation of this document, it is recommended to print it together with the ECSS-E-ST-20-20 and to consult Annex A, Annex B and Annex C separately and at the same time when reading the document core.

In this way, the discussion and the rationale explanation of each individual requirement are clearer and there is the minimum risk of misunderstanding.

5 Power distribution by LCLs/RLCLs

5.1 General architecture

A generic architecture for a Latching Current Limiter, or LCL, is shown in Figure 5-1.

Note that the diagram in Figure 5-1 is given only as a reference, without losing generality, and some of the features thereby reported can be actually realised differently.

Common LCL design alternatives are discussed further in section 5.2.

Without losing in generality, the general architecture is hereby explained for the distribution by LCLs.

For the specific case of Retriggerable Latching Current Limiter, or RLCL, refer to section 5.3.

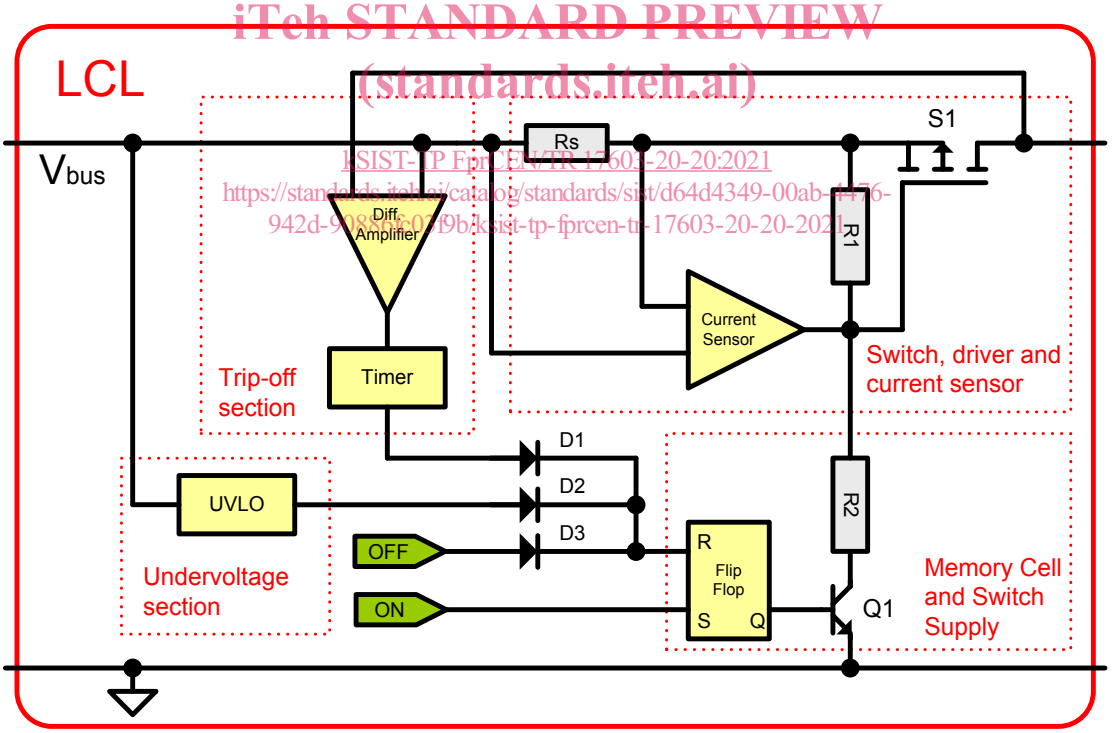

Figure 5-1: LCL generic block diagram

The Latching Current Limiter, or LCL, is a switch-able, latching, retriggerable over-current/overload protection placed between a power source and the relevant load.

The LCL can be commanded ON and OFF and its status is normally latched by a relevant memory cell.

Typically, an LCL presents a minimum residual resistance between power input and power output during nominal operation (i.e. when the switch is commanded closed).

In case of an overload, e.g. when the load current request exceeds a prefixed threshold, the LCL enters current limitation and a time counter is activated.

If the overload condition persists for a given time duration (called trip-off time), the time counter commands the LCL OFF.

Normally there should be an external command activation to reset the LCL into its original ON state.

Note that the LCL identifies a function: therefore it is independent from the number of power switches or MOSFETs used to implement the function itself.

The functionality of the LCL, in relation to the block diagram in Figure 5-1, is detailed in section 5.2.

5.2 Functionality

5.2.1 Overview

The basic elements of an LCL are the following:

- the section containing **the switch, the driver and the current sensor**,
- the section relevant to the **trip-off** timer,
- the section relevant to the **memory cell and switch supply** section,
- the **undervoltage protection** (UVP) section,
- the **auxiliary supply** section (not shown in Figure 5-1), and
- the **telemetry** section.

Each basic element is discussed in a dedicated section in the present chapter.

5.2.2 Switch, driver and current sensor

The switch is generally constituted by an enhancement MFET, either P or N channel, even though other devices could be used (for example, bipolar transistors for lower current applications).

It is called “switch” in relation to the switching capability of the LCL (e.g. it can apply or remove power from the load), but actually it operates either in ohmic “ON” mode or in linear mode according to the load current being below or above a specified threshold.