

---

---

**Identification cards — Test  
methods —**

**Part 3:  
Integrated circuit cards with contacts  
and related interface devices**

*Cartes d'identification — Méthodes d'essai —*

*Partie 3: Cartes à circuit(s) intégré(s) à contacts et dispositifs  
d'interface assimilés*

**Document Preview**

[ISO/IEC 10373-3:2018](https://standards.iteh.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018)

<https://standards.iteh.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018>



iTeh Standards  
(<https://standards.iteh.ai>)  
Document Preview

[ISO/IEC 10373-3:2018](https://standards.iteh.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018)

<https://standards.iteh.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018>



**COPYRIGHT PROTECTED DOCUMENT**

© ISO/IEC 2018

All rights reserved. Unless otherwise specified, or required in the context of its implementation, no part of this publication may be reproduced or utilized otherwise in any form or by any means, electronic or mechanical, including photocopying, or posting on the internet or an intranet, without prior written permission. Permission can be requested from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office  
CP 401 • Ch. de Blandonnet 8  
CH-1214 Vernier, Geneva  
Phone: +41 22 749 01 11  
Fax: +41 22 749 09 47  
Email: [copyright@iso.org](mailto:copyright@iso.org)  
Website: [www.iso.org](http://www.iso.org)

Published in Switzerland

# Contents

	Page
<b>Foreword</b> .....	<b>vi</b>
<b>1 Scope</b> .....	<b>1</b>
<b>2 Normative references</b> .....	<b>1</b>
<b>3 Terms and definitions</b> .....	<b>1</b>
<b>4 General items applicable to the test methods</b> .....	<b>2</b>
4.1 Test environment.....	2
4.2 Pre-conditioning.....	2
4.3 Selection of test methods.....	2
4.4 Default tolerance.....	3
4.5 Total measurement uncertainty.....	3
4.6 Conventions for electrical measurements.....	3
4.7 Apparatus.....	3
4.7.1 Apparatus for testing the integrated circuit cards with contacts (card-test-apparatus).....	3
4.7.2 Apparatus for testing the interface device (IFD-test-apparatus).....	6
4.7.3 Test Scenario.....	10
4.8 Relationship of test methods versus base standard requirements.....	10
<b>5 Test methods for electrical characteristics of cards with contacts</b> .....	<b>12</b>
5.1 VCC contact.....	12
5.1.1 General.....	12
5.1.2 Apparatus.....	12
5.1.3 Procedure.....	12
5.1.4 Test report.....	13
5.2 I/O contact.....	13
5.2.1 General.....	13
5.2.2 Apparatus.....	13
5.2.3 Procedure.....	13
5.2.4 Test report.....	14
5.3 CLK contact.....	14
5.3.1 General.....	14
5.3.2 Apparatus.....	14
5.3.3 Procedure.....	15
5.3.4 Test report.....	15
5.4 RST contact.....	15
5.4.1 General.....	15
5.4.2 Apparatus.....	16
5.4.3 Procedure.....	16
5.4.4 Test report.....	16
5.5 SPU (C6) contact.....	16
<b>6 Test methods for logical operations of cards with contacts</b> .....	<b>17</b>
6.1 Answer to reset.....	17
6.1.1 Cold reset and answer-to-reset (ATR).....	17
6.1.2 Warm reset.....	17
6.2 T=0 Protocol.....	18
6.2.1 General.....	18
6.2.2 I/O transmission timing for T=0 protocol.....	18
6.2.3 I/O character repetition for T=0 protocol.....	19
6.2.4 I/O reception timing and error signalling for T=0 protocol.....	19
6.3 T=1 Protocol.....	20
6.3.1 General.....	20
6.3.2 I/O transmission timing for T=1 protocol.....	20
6.3.3 I/O reception timing for T=1 protocol.....	21

6.3.4	Character Waiting Time (CWT) behaviour.....	22
6.3.5	Card-reaction to IFD exceeding CWT.....	22
6.3.6	Block Guard time (BGT).....	23
6.3.7	Block sequencing by the card.....	24
6.3.8	Reaction of the card to protocol errors.....	26
6.3.9	Recovery of a transmission error by the card.....	26
6.3.10	Resynchronization.....	27
6.3.11	IFSD negotiation.....	28
6.3.12	Abortion by the IFD.....	29
<b>7</b>	<b>Test methods for physical and electrical characteristics of the IFD.....</b>	<b>29</b>
7.1	Activation of contacts.....	29
7.1.1	General.....	29
7.1.2	Apparatus.....	29
7.1.3	Procedure.....	30
7.1.4	Test report.....	30
7.2	VCC contact.....	30
7.2.1	General.....	30
7.2.2	Apparatus.....	30
7.2.3	Procedure.....	30
7.2.4	Test report.....	31
7.3	I/O contact.....	32
7.3.1	General.....	32
7.3.2	Apparatus.....	32
7.3.3	Procedure.....	32
7.3.4	Test report.....	33
7.4	CLK contact.....	33
7.4.1	General.....	33
7.4.2	Apparatus.....	33
7.4.3	Procedure.....	33
7.4.4	Test report.....	34
7.5	RST contact.....	34
7.5.1	General.....	34
7.5.2	Apparatus.....	35
7.5.3	Procedure.....	35
7.5.4	Test report.....	36
7.6	SPU (C6) contact.....	36
7.7	Deactivation of the contacts.....	36
7.7.1	General.....	36
7.7.2	Apparatus.....	36
7.7.3	Procedure.....	36
7.7.4	Test report.....	36
<b>8</b>	<b>Test methods for logical operations of the IFD.....</b>	<b>37</b>
8.1	Answer to reset.....	37
8.1.1	Card reset (cold reset).....	37
8.1.2	Card reset (warm reset).....	37
8.2	T=0 Protocol.....	38
8.2.1	General.....	38
8.2.2	I/O transmission timing for T=0 protocol.....	38
8.2.3	I/O character repetition for T=0 protocol.....	38
8.2.4	I/O reception timing and error signaling for T=0 protocol.....	39
8.3	T=1 Protocol.....	40
8.3.1	General.....	40
8.3.2	I/O transmission timing for T=1 protocol.....	40
8.3.3	I/O reception timing for T=1 protocol.....	41
8.3.4	IFD Character Waiting Time (CWT) behaviour.....	42
8.3.5	IFD-reaction to card exceeding CWT.....	42
8.3.6	Block Guard Time (BGT).....	43

8.3.7	Block sequencing by the IFD .....	43
8.3.8	Recovery of a transmission error by the IFD .....	46
8.3.9	IFSC negotiation .....	47
8.3.10	Abortion by the card .....	47
8.4	IFD — Reaction of the IFD to invalid PCBs .....	48
8.4.1	General .....	48
8.4.2	Apparatus .....	48
8.4.3	Procedure .....	48
8.4.4	Test report .....	49
<b>Bibliography .....</b>		<b>50</b>

iTeh Standards  
 (https://standards.itih.ai)  
 Document Preview

[ISO/IEC 10373-3:2018](https://standards.itih.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018)

<https://standards.itih.ai/catalog/standards/iso/4350210b-0014-4b89-a39d-4b683e80e224/iso-iec-10373-3-2018>

## Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see [www.iso.org/directives](http://www.iso.org/directives)).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see [www.iso.org/patents](http://www.iso.org/patents)).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation on the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: [www.iso.org/iso/foreword.html](http://www.iso.org/iso/foreword.html).

This document was prepared by ISO/IEC JTC 1, *Information technology, SC 17, Cards and personal identification*.

This third edition cancels and replaces the second edition (ISO/IEC 10373-3:2010), which has been technically revised. It also incorporates the Technical Corrigendum ISO/IEC 10373-3:2010/Cor 1:2013.

The main changes compared to the previous edition are as follows:

- editorial clarification of scenario 6 (6.3.6.2.3 in the previous edition) with addition of supported PCB values;
- miscellaneous editorial improvement on e.g. symbols, notes and references.

A list of all the parts in the ISO 10373 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at [www.iso.org/members.html](http://www.iso.org/members.html).

# Identification cards — Test methods —

## Part 3:

# Integrated circuit cards with contacts and related interface devices

## 1 Scope

This document defines test methods for characteristics of integrated circuit cards with contacts and related interface devices according to the definition given in ISO/IEC 7816-3. Each test method is cross-referenced to one or more base standards, which can be ISO/IEC 7810 that defines the information storage technologies employed in identification card applications.

NOTE Criteria for acceptability do not form part of this document but can be found in the International Standards mentioned above.

This document defines test methods which are specific to integrated circuit technology with contacts. ISO/IEC 10373-1 defines test methods which are common to one or more card technologies and other parts of the ISO/IEC 10373 series define other technology-specific tests.

Test methods defined in this document are intended to be performed separately and independently. A given card is not required to pass through all the tests sequentially. The test methods defined in this document are based on ISO/IEC 7816-3.

Conformance of cards and IFDs determined using the test methods defined in this document does not preclude failures in the field. Reliability testing is outside the scope of this document.

This document does not define any test to establish the complete functioning of integrated circuit cards. The test methods require only that the minimum functionality be verified. The minimum functionality is defined as follows.

- Any integrated circuit present in the card continues to show an Answer to Reset response which conforms to the base standard.
- Any contacts associated with any integrated circuit present in the card continue to show electrical resistance which conforms to the base standard.

## 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7816-3:2006, *Identification cards — Integrated circuit cards — Part 3: Cards with contacts — Electrical interface and transmission protocols*

## 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at <https://www.iso.org/obp>

— IEC Electropedia: available at <http://www.electropedia.org/>

**3.1**  
**card**  
integrated circuit card with contacts

**3.2**  
**DUT**  
device under test  
*card* (3.1) or *IFD* (3.4) that is subject to testing

**3.3**  
**etu-factor**  
parameters negotiable by protocol and parameters selection (PPS), described in ISO/IEC 7816-3:2006, 6.3.1

**3.4**  
**IFD**  
interface device related to integrated circuit cards with contacts as defined in ISO/IEC 7816-3

**3.5**  
**normal use**  
use as an identification card, involving equipment processes appropriate to the card technology and storage as a personal document between equipment processes

[SOURCE: ISO/IEC 7810:2003, 4.4]

**3.6**  
**test method**  
method for testing characteristics of identification cards and related interface devices for the purpose of confirming their compliance with International Standards

**3.7**  
**test scenario**  
defined typical protocol and application specific communication to be used with the *test methods* (3.6) defined in this document

**3.8**  
**typical protocol and application specific communication**  
communication between a *DUT* (3.2) and the corresponding test-apparatus based on the protocol and application implemented in the *DUT* (3.2) and representing its *normal use* (3.5)

## 4 General items applicable to the test methods

### 4.1 Test environment

Unless otherwise specified, testing of physical, electrical and logical characteristics shall take place in an environment of a temperature  $23\text{ °C} \pm 3\text{ °C}$ , of a relative humidity 40 % to 60 %.

### 4.2 Pre-conditioning

Where pre-conditioning is required by the test method, the identification cards to be tested shall be conditioned to the test environment for a period of 24 h before testing unless otherwise specified.

### 4.3 Selection of test methods

Tests shall be applied as required to test the attributes of the card defined by the relevant base standard (see 4.8).



#### 4.4 Default tolerance

Unless otherwise specified, a default tolerance of  $\pm 5\%$  shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

#### 4.5 Total measurement uncertainty

The total measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

#### 4.6 Conventions for electrical measurements

Potential differences are defined with respect to the GND contact of the card and currents flowing to the card are considered positive.

#### 4.7 Apparatus

##### 4.7.1 Apparatus for testing the integrated circuit cards with contacts (card-test-apparatus)

##### 4.7.1.1 Generating the VCC voltage ( $U_{CC}$ ) and timing

Table 1 — Voltage and timing for VCC

Parameter	Operating condition	Range	Accuracy
$U_{CC}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV
$t_R, t_F$	Class A, B, C	0 $\mu$ s to 500 $\mu$ s	$\pm 100$ $\mu$ s

##### 4.7.1.2 Measuring ICC

Table 2 —  $I_{CC}$  parameters

Characteristic	Mode	Range	Accuracy	Resolution
$I_{CC}$	Spike measurement	0 mA to 200 mA	$\pm 2$ mA	20 ns
	Active mode	0 mA to 100 mA	$\pm 1$ mA	Averaged over 1 ms
	Clock stop	0 $\mu$ A to 200 $\mu$ A	$\pm 10$ $\mu$ A	Averaged over 1 ms

##### 4.7.1.3 Generating SPU (C6) voltage

See 5.5 and ISO/IEC 7816-3.

##### 4.7.1.4 Generating the RST voltage and timing

Table 3 — RST voltage and timing

Parameter	Operating condition	Range	Accuracy
$U_{IH}, U_{IL}$	Class A, B	-1 V to 6 V	$\pm 20$ mV
$U_{IH}$	Class C	-1 V to 2 V	$\pm 20$ mV
$U_{IL}$	Class C	-1 V to 1 V	$\pm 20$ mV
$t_R, t_F$		0 $\mu$ s to 2 $\mu$ s	$\pm 20$ ns
NOTE $t_R$ and $t_F$ are generated between 10 % and 90 % of the $V_H$ min and $V_L$ max values.			

## 4.7.1.5 Measuring the RST current

Table 4 — RST current

Characteristic	Mode	Range	Accuracy	Resolution
$I_{IH}$	Active	-30 $\mu$ A to 200 $\mu$ A	$\pm 10$ $\mu$ A	100 ns
$I_{IL}$	Active	-200 $\mu$ A to 30 $\mu$ A	$\pm 10$ $\mu$ A	100 ns

## 4.7.1.6 Generating the I/O voltage and timing in reception mode

Table 5 — I/O voltage and timing

Parameter	Mode	Operating condition	Range	Accuracy
$U_{IH}, U_{IL}$	Card: Reception, Apparatus: Transmission	Class A, B	-1 V to 6 V	$\pm 20$ mV
$U_{IH}$	Card: Reception, Apparatus: Transmission	Class C	-1 V to 2 V	$\pm 20$ mV
$U_{IL}$	Card: Reception, Apparatus: Transmission	Class C	-1 V to 1 V	$\pm 20$ mV
$t_R, t_F$	Card: Reception, Apparatus: Transmission		0 $\mu$ s to 2 $\mu$ s	$\pm 100$ ns

NOTE  $t_R$  and  $t_F$  are generated between 10 % and 90 % of the  $V_H$  min and  $V_L$  max values.

## 4.7.1.7 Measuring the I/O current in reception mode

Table 6 — I/O current (reception mode)

Parameter	Mode	Range	Accuracy	Resolution
$I_{IH}$	Card: Reception, Apparatus: Transmission	-300 $\mu$ A to 30 $\mu$ A	$\pm 10$ $\mu$ A	100 ns
$I_{IL}$	Card: Reception, Apparatus: Transmission	-1,5 mA to -0,2 mA	$\pm 50$ $\mu$ A	100 ns
	Card: Reception, Apparatus: Transmission	-200 $\mu$ A to 30 $\mu$ A	$\pm 10$ $\mu$ A	100 ns

## 4.7.1.8 Generating the I/O current

Table 7 — I/O current

Parameter	Mode	Range	Accuracy	Stabilization time after level is reached
$I_{OH}$	Card: Transmission Apparatus: Reception	20 k $\Omega$ pull-up to VCC or equivalent circuit	$\pm 200$ $\Omega$	
$I_{OL}$	Card: Transmission Apparatus: Reception	0 mA to 1,5 mA	$\pm 50$ $\mu$ A	<100 ns

## 4.7.1.9 Measuring the I/O voltage and timing

Table 8 — I/O voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{IH}, U_{IL}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	20 ns
$t_R, t_F$		0 $\mu$ s to 2 $\mu$ s	$\pm 20$ ns	

NOTE  $t_R$  and  $t_F$  are measured between 10 % and 90 % of the  $V_H$  min and  $V_L$  max values.

## 4.7.1.10 Generating the CLK voltage

Table 9 — CLK voltage

Parameter	Operating condition	Range	Accuracy	Resolution
$U_{IH}, U_{IL}$	Class A, B	-1 V to 6 V	±20 mV	20 ns
$U_{IH}$	Class C	-1 V to 2 V	±20 mV	20 ns
$U_{IL}$	Class C	-1 V to 2 V	±20 mV	20 ns

## 4.7.1.11 Generating the CLK waveforms (single cycle measurement)

Table 10 — CLK waveforms

Parameter	Range	Accuracy
Duty cycle	35 % to 65 % of period	±5 ns
Frequency	0,5 MHz to 5,5 MHz	±5 kHz
Frequency	5 MHz to 20,5 MHz	±50 kHz
$t_R, t_F$	1 % to 10 % of period	±5 ns

NOTE  $t_R$  and  $t_F$  are generated between 10 % and 90 % of the  $V_H$  (100 %) min and  $V_L$  (0 %) max.

## 4.7.1.12 Measuring the CLK current

Table 11 — CLK current

Characteristic	Mode	Range	Accuracy	Resolution
$I_{IH}$	Active	-30 $\mu$ A to 150 $\mu$ A	±10 $\mu$ A	20 ns
$I_{IL}$	Active	-150 $\mu$ A to 30 $\mu$ A	±10 $\mu$ A	20 ns

## 4.7.1.13 Measuring the contact capacitance of RST, CLK and I/O

The contact capacitance of a contact shall be measured between the contact and the GND contact.

Table 12 — Contact capacitance

Characteristic	Range	Accuracy
C	0 pF to 50 pF	±5 pF

## 4.7.1.14 Generating the sequence of the activation and deactivation of the contacts

Table 13 — Activation and deactivation

Range of switching the signals	Accuracy
0 s to 1 s	±200 ns (or 1 CLK period, whichever is smaller)

## 4.7.1.15 Emulating the I/O protocol

The card-test-apparatus shall be able to emulate the protocol T=0 and T=1 and IFD applications which are required to run the typical application specific communications corresponding to the card applications.

NOTE If a specific functionality is not implemented in the card, the card-test-apparatus is not required to have the corresponding test-capability (e.g. T=1 protocol not implemented in the card).

**4.7.1.16 Generating the I/O character timing in reception mode**

The card-test-apparatus shall be able to generate the I/O bit stream according to ISO/IEC 7816-3.

All timing parameters, e.g. start bit length, guard time, error signaling, shall be configurable.

**Table 14 — I/O character timing (reception mode)**

Symbol	Parameter	Accuracy
$\epsilon_t$	All timing parameters	$\pm 4$ CLK cycles

**4.7.1.17 Measuring and monitoring the I/O protocol**

The card-test-apparatus shall be able to measure and monitor the timing of the logical low and high states of the I/O-line relative to the CLK-frequency.

**Table 15 — Timing characteristics**

Characteristic	Accuracy
All timing characteristics	$\pm 2$ CLK cycles

**4.7.1.18 Protocol analysis**

The card-test-apparatus shall be able to analyse the I/O-bit stream in accordance to T=0 and T=1 protocol according to ISO/IEC 7816-3 and extract the logical data flow for further protocol and application verifications.

NOTE If a specific functionality is not implemented in the card, the card-test-apparatus is not required to have the corresponding test-capability (e.g. T=1 protocol not implemented in the card). Conversely, it is possible that an apparatus needs extended capabilities, e.g. being able to generate any case 2 command (see ISO/IEC 7816-4) if a card does not support the standard READ BINARY.

**4.7.2 Apparatus for testing the interface device (IFD-test-apparatus)**

**4.7.2.1 Generating the VCC current ( $I_{CC}$ )**

**Table 16 — VCC current**

Parameter	Mode	Range	Accuracy	Stabilization time after the level is reached
$I_{CC}$	Spike generation	0 mA to 120 mA	$\pm 2$ mA <sup>b</sup>	<100 ns
	Active mode	0 mA to 70 mA	$\pm 1$ mA	<100 ns
	Idle mode (CLK-Stop)	0 mA to 1,2 mA	$\pm 10$ $\mu$ A	<100 ns
	Inactive <sup>a</sup>	-1,2 mA to 0 mA	$\pm 10$ $\mu$ A	<100 ns
$t_R, t_F$		100 ns	$\pm 50$ ns	
pulse length		100 ns to 500 ns	$\pm 50$ ns	
pause length frequently		100 ns to 1 000 ns	$\pm 50$ ns	
pause length randomly		10 $\mu$ s to 2 000 $\mu$ s	$\pm 1$ $\mu$ s	

<sup>a</sup> The maximum output voltage shall be limited to 5 V.

<sup>b</sup> Dynamic conditions for spike generation.

4.7.2.2 Measuring the VCC voltage ( $U_{CC}$ ) and timing

Table 17 — VCC voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{CC}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	10 ns

4.7.2.3 Measuring the SPU (C6) voltage ( $U_{CC}$ ) and timing

Table 18 — SPU voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{CC}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	10 ns

## 4.7.2.4 Generating the RST current

Table 19 — RST current

Parameter	Mode	Range	Accuracy	Stabilization time after the level is reached
$I_{IH}$	Active	-30 $\mu$ A to 200 $\mu$ A	$\pm 10$ $\mu$ A	<100 ns
$I_{IL}$	Active	-250 $\mu$ A to 30 $\mu$ A	$\pm 10$ $\mu$ A	<100 ns
$I^a$	Inactive	-1,2 mA to 0 mA	$\pm 10$ $\mu$ A	<100 ns

<sup>a</sup> The output voltage shall be limited to a range from -0,5 V to 5,5 V.

## 4.7.2.5 Measuring RST voltage and timing

Table 20 — RST voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{IH}, U_{IL}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	20 ns
$t_R, t_F$		0 $\mu$ s to 2 $\mu$ s	$\pm 20$ ns	

NOTE  $t_R$  and  $t_F$  are measured between 10 % and 90 % of the  $V_H$  min and  $V_L$  max values.

## 4.7.2.6 Generating the I/O currents

Table 21 — I/O currents

Parameter	Mode	Range	Accuracy	Stabilization time after the level is reached
$I_{IH}, I_{OH}$	Apparatus: Reception and Transmission IFD: Transmission and Reception	-400 $\mu$ A to 50 $\mu$ A	$\pm 5$ $\mu$ A	<100 ns
$I_{IL}$	Apparatus: Reception IFD: Transmission and Reception	0 mA to 1,5 mA	$\pm 10$ $\mu$ A	<100 ns
$I_{OL}$	IFD: Reception	0 $\mu$ A to 1 200 $\mu$ A	$\pm 10$ $\mu$ A	<100 ns
$I^a$	Inactive	-1,2 mA to 0 mA	$\pm 10$ $\mu$ A	<100 ns

<sup>a</sup> The output voltage shall be limited to a range from -0,5 V to 5,5 V.

## 4.7.2.7 Measuring the I/O voltage and timing

Table 22 — I/O voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{IH}, U_{IL}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	20 ns
$t_R, t_F$		0 $\mu$ s to 2 $\mu$ s	$\pm 20$ ns	

NOTE  $t_R$  and  $t_F$  are measured between 10 % and 90 % of the  $V_H$  min and  $V_L$  max values.

## 4.7.2.8 Generating the I/O voltage and timing in transmission mode

Table 23 — I/O voltage and timing (transmission mode)

Parameter	Mode	Operating condition	Range	Accuracy
$U_{IH}, U_{IL}$	IFD: Reception, Apparatus: Transmission	Class A, B	-1 V to 6 V	$\pm 20$ mV
$U_{IH}$	IFD: Reception, Apparatus: Transmission	Class C	-1 V to 2 V	$\pm 20$ mV
$U_{IL}$	IFD: Reception, Apparatus: Transmission	Class C	-1 V to 1 V	$\pm 20$ mV
$t_R, t_F$	IFD: Reception, Apparatus: Transmission		0 $\mu$ s to 2 $\mu$ s	$\pm 100$ ns

NOTE  $t_R$  and  $t_F$  are generated between 10 % and 90 % of the  $V_H$  min and  $V_L$  max values.

## 4.7.2.9 Measuring the I/O current in transmission mode

Table 24 — I/O current (transmission mode)

Parameter	Mode	Range	Accuracy	Resolution
$I_{OL}$	Transmission	0 $\mu$ A to 1 200 $\mu$ A	$\pm 10$ $\mu$ A	20 ns
$I_a$	Inactive	0 mA to 1,2 mA	$\pm 10$ $\mu$ A	20 ns

<sup>a</sup> The output voltage shall be limited to a range from -0,5 V to 5,5 V.

## 4.7.2.10 Generating the CLK current

Table 25 — CLK current

Parameter	Mode	Range	Accuracy	Stabilization time after the level is reached
$I_{IH}$	Active	-30 $\mu$ A to 150 $\mu$ A	$\pm 10$ $\mu$ A	<20 ns
$I_{IL}$	Active	-150 $\mu$ A to 30 $\mu$ A	$\pm 10$ $\mu$ A	<20 ns
$I_a$	Inactive	-1,2 mA to 0 mA	$\pm 10$ $\mu$ A	<100 ns

<sup>a</sup> The output voltage shall be limited to -0,5 V to 5,5 V.

## 4.7.2.11 Measuring the CLK voltage and timing

Table 26 — CLK voltage and timing

Characteristic	Operating condition	Range	Accuracy	Resolution
$U_{IH}, U_{IL}$	Class A, B, C	-1 V to 6 V	$\pm 20$ mV	20 ns