SLOVENSKI STANDARD
oSIST prEN IEC 60749-34-1:2024

01-februar-2024

Polprevodniški elementi - Mehanske in klimatske preskusne metode - 34-1. del: Preskus močnostnega polprevodniškega modula s cikliranjem električnega napajanja

Semiconductor devices - Mechanical and climatic test methods - Part 34-1: Power cycling test for power semiconductor module

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 34 -1: Essai de cycles en puissance pour modules de puissance à semiconducteurs

Ta slovenski standard je istoveten z: **prEN IEC 60749-34-1:2023**

ICS:

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COMMITTEE DRAFT FOR VOTE (CDV)

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IEC TC 47 : SEMICONDUCTOR DEVICES

SECRETARIAT:	SECRETARY:
Korea, Republic of	Mr Cheolung Cha
OF INTEREST TO THE FOLLOWING COMMITTEES:	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.

FUNCTIONS CONCERNED:

☐ EMC ☐ ENVIRONMENT ☒ QUALITY ASSURANCE ☐ SAFETY

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TITLE:

Semiconductor devices - Mechanical and climatic test methods - Part 34-1: Power cycling test for power semiconductor module

PROPOSED STABILITY DATE: 2029

NOTE FROM TC/SC OFFICERS:

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 34-1: Power cycling test for power semiconductor module

FOREWORD

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International Standard IEC 60749 has been prepared by IEC technical committee TC47.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/XX/FDIS	47/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at

www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at http://www.iec.ch/standardsdev/publications.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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INTRODUCTION

A power semiconductor module is affected by thermal and mechanical stress due to the power dissipation of the internal semiconductor dies and connectors. This occurs when low-voltage operating bias for forward conduction is periodically applied and removed, causing rapid changes in temperature. The power cycling test is intended to simulate the temperature swing in typical power electronics applications, which is different from the stable temperatures reached under the HTOL test (High Temperature Operating Life) (see IEC 60749-23). Exposure to the power cycling test may not induce the same failure mechanisms as exposure to the thermal cycling test, or thermal shock test. The power cycling test is a destructive test that will cause wear-out failure of the DUT if it is driven above the specification of the device.

The power cycling test is applied to general power semiconductor modules such as for example those used for motor control, robots, and renewable energy generation. The power cycling test has two modes: a short-time test (based on a short cycle time) that simulates rapid acceleration and deceleration of the equipment, and a long-time test (based on a long cycle time) that simulates repeated operation and stop of the equipment. The short-time test mainly verifies the effect of the temperature change of Tvj, and causes the deterioration of the joint between the semiconductor die and the wire, and that of the die attach under the semiconductor die. The long-time test verifies the effect of the temperature change of Tc, and causes the deterioration of the joining layer between the metallic base plate and the insulating substrate, and the deterioration of the die attach under the semiconductor die.

The power cycling test is performed in two cases: as a certification test for the products whose power cycling lifetime model has already been confirmed, and as a lifetime model validation test for the products whose lifetime model has not been confirmed. The purpose of the certification test is to verify that the product has a longer life than the specified number of cycles.

Moreover, the purpose of the lifetime model validation test is to statistically estimate the power cycling lifetime model from the test results, and obtain the expected lifetime model of power modules. This is required when customers design the lifetime of their products.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 34-1: Power cycling test for power semiconductor module

1 Scope

This part of IEC IEC 60749 describes a test method that is used to determine the capability of power semiconductor modules to withstand thermal and mechanical stress resulting from cycling the power dissipation of the internal semiconductors and the internal connectors. It is based on IEC 60749-34, Power cycling, but is developed specifically for silicon-based power semiconductor module products.

This test causes wear-out and is considered destructive.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-4, Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages

IEC 60747-2, Semiconductor devices – Part 2: Discrete devices – Rectifier diodes

IEC 60747-6, Semiconductor devices – Part 6: Discrete devices – Thyristors

IEC 60747-8, Semiconductor devices – Discrete devices – Part 8: Field-effect transistors

IEC 60747-9, Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)

IEC 60747-15, Semiconductor devices – Discrete devices – Part 15: Isolated power semiconductor devices

IEC 60749-34, Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

NOTE Further terms and definitions pertaining to semiconductor devices can be found in the IEC 60747 and IEC 60749 series.

3.1
power semiconductor module

isolated or non-isolated semiconductor module with two or more semiconductor dies according to the package outline style code “MP” specified in IEC 60191-4

Note 1 to entry: The predominantly used package body material is plastic (including epoxy) according to IEC 60191-4 and both the frame based and resin based embodiment are possible.

3.2
device under test
DUT

188 device to be teste

189 **3.3**
190 **case temperature**
191 T_c

192 case surface temperature directly below the power semiconductor module under test

193 **3.4**
194 **junction temperature excursion**
195 ΔT_{vj}

196 difference between virtual maximum and minimum junction temperature of the DUT during one power
197 cycle

198 **3.5**
199 **case temperature excursion**
200 ΔT_c

201 difference between maximum and minimum case temperature during one power cycle

202 **3.6**
203 **minimum virtual junction temperature**
204 $T_{vj,min}$

205 minimum virtual junction temperature of the DUT

206 **3.7**
207 **maximum virtual junction temperature**
208 $T_{vj,max}$

209 maximum virtual junction temperature of the DUT

210 **3.8**
211 **minimum case temperature**
212 $T_{c,min}$

213 minimum case surface temperature directly below the power semiconductor module under test

214 **3.9**
215 **maximum case temperature**
216 $T_{c,max}$

217 maximum case surface temperature directly below the power semiconductor module under test

218 **3.10**
219 **on-time**
220 t_{on}

221 time interval during which the DUT under test is conducting load current

222 **3.11**
223 **off-time**
224 t_{off}

225 time interval for cooling down

226 **3.12**
227 **cycle period**
228 sum of on-time and off-time