SLOVENSKI STANDARD
oSIST prEN IEC 63419:2022

01-april-2022

Smernice za postopke ocenjevanja stikalne zanesljivosti galij-nitridnih razsmernikov

Guideline for Switching Reliability Evaluation procedures for Gallium Nitride Power Conversion Devices

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Guideline for Switching Reliability Evaluation procedures for Gallium Nitride Power Conversion Devices

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This document is allocated to TC 47 / WG 8 and the project leader is Dr Stephanie Watts Butler.

This document is also of interest to TC 47/WG 5.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES

FOREWORD

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Draft	Report on voting
XX/XX/FDIS	XX/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This document is intended for use by GaN product suppliers and related power electronic industries. It provides guidelines for evaluating the switching reliability of GaN power switches and assuring their reliable use in power conversion applications. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches.

Gallium Nitride (GaN) power switches are important devices for high-efficiency, small form-factor power conversion applications. Current GaN power switches are based upon the planar High Electron Mobility Transistor (HEMT), which is a Field-Effect Transistor (FET). The switch can be a discrete enhancement or depletion-mode GaN FET, a GaN FET in combination with a silicon transistor forming a cascode and/or co-packaged with silicon control electronics. It can also be a GaN power FET with integrated GaN electronics. During operation, all power devices experience switching stress for which the reliability needs to be evaluated and lifetimes assured.

For many silicon power conversion products, operational robustness is often validated by a combination of technology and product-level tests, e.g., Hot Carrier Injection (HCI) [1], Unclamped Inductive Switching (UIS) [2], high-temperature operating life (HTOL) [3]. Individual silicon tests do not necessarily validate operation under actual-use conditions of power conversion products, which simultaneously involve high power transfer through the device, high slew rates, and hot-carrier effects. Each addresses different aspects, and over the years they have been developed to work well together. These tests are either not applicable or have not been comprehensively specified for GaN switches. For example, the HCI test relies on a body contact that is not available in GaN FETs and the UIS test takes the device into avalanche, which is not recommended for GaN FETs. The GaN industry has therefore been conducting switching reliability testing to assure the reliability and robustness of GaN switches [4]-[8], both at the technology level and in application.

The industry and research community now need to work towards standardizing the methodology for assuring both the switching reliability of the technology platform and the robustness of GaN switches for use in a broad class of power management applications. Typically, standards lag technology introduction because there needs to be substantial public knowledge of failure modes and mechanisms before a standards document can be published. This takes time because confidential information needs to be de-classified and new knowledge discovered. It is, however, desirable for the industry to develop common approaches sooner, so that customers can readily evaluate the technology options available. The goal of this document is to present guidelines for a common approach, and to accelerate progress towards the future standard.

A common approach for power management needs to consider many aspects. Power conversion involves different modes of operation, e.g., hard and soft-switching, the usage of the power switch in many different topologies, and the interaction of the switch with other system components. The approach also needs to detect failure modes of interest to the power electronics industry, e.g., lower efficiency from an increase in on-resistance [7]. It also needs to consider the limitations and strengths of classes of boards and hardware in conducting the stress-testing needed. Finally, the approach needs to assure broad coverage, so as not to introduce unnecessary burden on the industry.

This document provides a common approach for assuring that GaN products are reliable in power conversion applications. It provides guidelines for broad coverage, addresses the detection of relevant failure modes, provides guideline stress-test procedures, and proposes common ways to collect and present data. The approach is broken down into guidelines for the three key aspects as shown in Figure 1.

1) A procedure for obtaining broad coverage by classifying the switching stress stimuli with their switching loci and explaining the use of a harsher stress condition to cover a milder use-case condition.

2) A procedure for obtaining the switching lifetime of the technology platform. This involves performing accelerated life testing with a suitable type of GaN die or core switch to generate a model.

3) A procedure for validating reliable operation under application-use conditions by running parts in an application environment using stress conditions that, if passing, would assure reliable operation for a broad range of use-conditions.

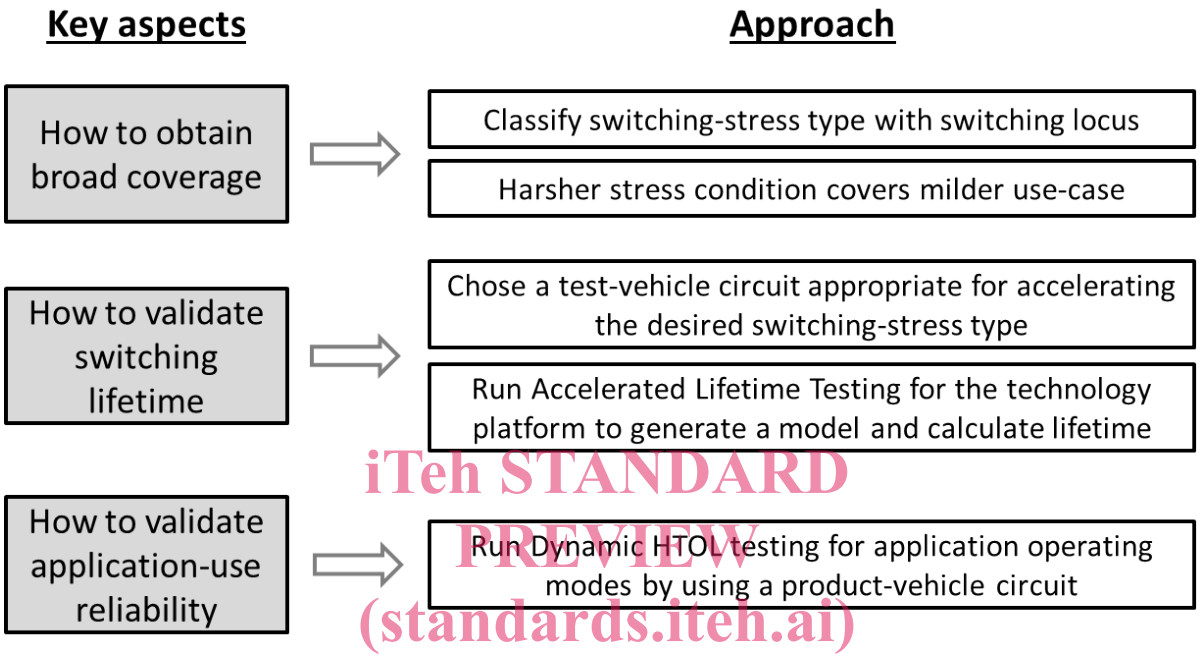

Figure 1 — Simplified explanation of the approach for assuring GaN product reliability. It consists of three key aspects as shown. The approach is not intended to be restrictive, as is described in the text

The approach is not intended to be restrictive. It takes into account the strengths and limitations of boards, hardware, and components, while also recognizing the need to not introduce unnecessary burden on the industry. It does not restrict additional testing, larger sample sizes, and stress conditions with higher acceleration. It also does not restrict the use of boards and device types. For instance, lifetime determination can be made using more complex boards or GaN switches by verifying that the complexity does not mask the acceleration of relevant failure mechanisms. Conversely simpler boards can be used to assure application-use reliability by providing collateral material showing robustness to operating modes not tested.

The core of this guideline is organized into four clauses, with clauses 5-7 reflective of the aspects of Figure 1.

– Clause 4 gives general guidance for selecting test devices, test circuits and developing test plans.
– Clause 5 provides an approach for broad coverage by using the switching locus curve.
– Clause 6 gives the procedure for obtaining wearout models and device lifetime.
– Finally, clause 7 provides guidance on validating reliable operation of GaN switches in power conversion applications.

1 Scope

This publication presents guidelines for evaluating the switching reliability of GaN power switches. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches. It covers the following aspects:

a) An approach for broad coverage, using the switching locus to represent switching stress in a standardized manner.

b) The development of a lifetime model, based upon the type of application switching locus.

c) The validation of reliable operation under application-use conditions.

The publication will result in common methods for representing, evaluating and modeling the switching stress on GaN power switches, and ensuring their reliable operation in an application.

2 Normative references

JEDEC JEP173, *Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, Version 1.0*, January 2019

To add: upon publication: IEC 63284 ED1, *Semiconductor devices – Reliability test method by inductive load switching for gallium nitride transistors*

3 Terms, definitions, symbols and abbreviated terms

No terms and definitions are listed in this document. ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

Symbol or Abbreviation	Name or term
$R_{DS(ON)}$	Drain to Source Resistance of DUT in ON-state
V_T	Threshold Voltage
i_D	Drain current of the DUT, time varying
v_{DS}	Drain to Source Voltage of DUT, time varying
I_D	Drain current in on-state of DUT
V_{DS}	Drain to Source Voltage of DUT
I_{DP}	Drain current parameter to represent the switching stress
V_{DP}	Drain voltage parameter to represent the switching stress
MTTF	Mean Time To Failure for a set of stress conditions
ttf	Times To Failure
E_A	Activation Energy
T_J	Junction Temperature of DUT
T_C	Case Temperature of DUT
$R_{\theta JC}$	Thermal resistance from device junction to case
f_{SW} D	Switching Frequency Duty cycle
t_r	Rise Time of VDS while switching
t_f	Fall Time of VDS while switching

Symbol or Abbreviation	Name or term
$f_{v, i, T, etc}$	Acceleration function for given stressor
AF	Acceleration Factor
K1, K2, K3, K4	Constants in empirical acceleration models
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
FET	Field Effect Transistor
HTOL	High Temperature Operating Life
UIS	Unclamped Inductive Switching
HCI	Hot Carrier Injection
DOE	Design of Experiments
SALT	Switching Accelerated Life Test
DHTOL	Dynamic High Temperature Operating Life
DUT	Device Under Test
PCB	Printed Circuit Board
HTRB	High Temperature Reverse Bias
ZCS	Zero Current Switched
ZVS	Zero Voltage Switched

4 Description of test elements

4.1 Objectives of stress testing for switching reliability

There are two classes of stress tests recommended in this guideline: Switching Accelerated Life Test (Switching-ALT or SALT) and Dynamic High-Temperature Operating-Life (DHTOL) test.

For an accelerated lifetime test such as SALT, stress conditions are typically chosen such that there will be wearout failures in the test timeframe. Failures are needed to allow the plotting of failure distributions, e.g., Weibull, lognormal, etc. Wearout models are obtained using these distributions and allow calculation of the device lifetime for application-use conditions. Further details about lifetime determination using SALT are provided in clause 6.

For DHTOL, stress conditions are chosen to represent the most stringent mission profile so as to cover all different application use cases, as described further in clauses 5 and 7. DHTOL conditions are typically not chosen to stress till wearout, and it is expected that there will be no failures in the test timeframe. Industry best-practice conditions are used in cases where GaN-specific knowledge is not yet available. An example of best-practice conditions in use for silicon discrete power FETs is the application of stress at 80% of the device rating (or absolute maximum voltage), or at 100% of the maximum recommended voltage (if specified) and the maximum recommended temperature for 1000h.