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Smernice za postopke ocenjevanja stikalne zanesljivosti galij-nitridnih razsmernikov

Guideline for Switching Reliability Evaluation procedures for Gallium Nitride Power Conversion Devices

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This CDV is based upon JEDEC document JEP180 (title: Guideline for Switching Reliability Evaluation procedures for Gallium Nitride Power Conversion Devices) and is circulated according to the IEC fast-track procedure (see F.2 of ISO/IEC Directives, Part 1, 2021).

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This document is allocated to TC 47 / WG 8 and the project leader is Dr Stephanie Watts Butler.

This document is also of interest to TC 47/WG 5.

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

114 The language used for the development of this International Standard is English.

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- 122 reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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INTRODUCTION

This document is intended for use by GaN product suppliers and related power electronic industries. It provides guidelines for evaluating the switching reliability of GaN power switches and assuring their reliable use in power conversion applications. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches.

136 Gallium Nitride (GaN) power switches are important devices for high-efficiency, small formfactor power conversion applications. Current GaN power switches are based upon the planar 137 High Electron Mobility Transistor (HEMT), which is a Field-Effect Transistor (FET). The switch 138 can be a discrete enhancement or depletion-mode GaN FET, a GaN FET in combination with a 139 silicon transistor forming a cascode and/or co-packaged with silicon control electronics. It can 140 also be a GaN power FET with integrated GaN electronics. During operation, all power devices 141 experience switching stress for which the reliability needs to be evaluated and lifetimes 142 assured. 143

For many silicon power conversion products, operational robustness is often validated by a 144 combination of technology and product-level tests, e.g., Hot Carrier Injection (HCI) [1], 145 Unclamped Inductive Switching (UIS) [2], high-temperature operating life (HTOL) [3]. Individual 146 silicon tests do not necessarily validate operation under actual-use conditions of power 147 conversion products, which simultaneously involve high power transfer through the device, high 148 slew rates, and hot-carrier effects. Each addresses different aspects, and over the years they 149 have been developed to work well together. These tests are either not applicable or have not 150 been comprehensively specified for GaN switches. For example, the HCI test relies on a body 151 contact that is not available in GaN FETs and the UIS test takes the device into avalanche, 152 153 which is not recommended for GaN FETs. The GaN industry has therefore been conducting switching reliability testing to assure the reliability and robustness of GaN switches [4]-[8], both 154 at the technology level and in application. 155

156 The industry and research community now need to work towards standardizing the methodology for 157 assuring both the switching reliability of the technology platform and the robustness of GaN switches for use in a broad class of power management applications. Typically, standards lag technology 158 introduction because there needs to be substantial public knowledge of failure modes and mechanisms 159 before a standards document can be published. This takes time because confidential information needs 160 to be de-classified and new knowledge discovered. It is, however, desirable for the industry to develop 161 common approaches sooner, so that customers can readily evaluate the technology options available. 162 The goal of this document is to present guidelines for a common approach, and to accelerate progress 163 towards the future standard. 164

A common approach for power management needs to consider many aspects. Power conversion involves different modes of operation, e.g., hard and soft-switching, the usage of the power switch in many different topologies, and the interaction of the switch with other system components. The approach also needs to detect failure modes of interest to the power electronics industry, e.g., lower efficiency from an increase in on-resistance [7]. It also needs to consider the limitations and strengths of classes of boards and hardware in conducting the stress-testing needed. Finally, the approach needs to assure broad coverage, so as not to introduce unnecessary burden on the industry.

This document provides a common approach for assuring that GaN products are reliable in power conversion applications. It provides guidelines for broad coverage, addresses the detection of relevant failure modes, provides guideline stress-test procedures, and proposes common ways to collect and present data. The approach is broken down into guidelines for the three key aspects as shown in Figure 1.

A procedure for obtaining broad coverage by classifying the switching stress stimuli with
 their switching loci and explaining the use of a harsher stress condition to cover a milder
 use-case condition.

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- A procedure for obtaining the switching lifetime of the technology platform. This involves
 performing accelerated life testing with a suitable type of GaN die or core switch to
 generate a model.
- A procedure for validating reliable operation under application-use conditions by running
 parts in an application environment using stress conditions that, if passing, would assure
 reliable operation for a broad range of use-conditions.

Key aspects

Approach



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Figure 1 — Simplified explanation of the approach for assuring GaN product reliability. It consists of three key aspects as shown. The approach is not intended to be restrictive, as is described in the text bba2-49ad-95e0-4210180e0ac/05181-pren-iec-63419-

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The approach is not intended to be restrictive. It takes into account the strengths and limitations of 191 boards, hardware, and components, while also recognizing the need to not introduce unnecessary 192 burden on the industry. It does not restrict additional testing, larger sample sizes, and stress conditions 193 with higher acceleration. It also does not restrict the use of boards and device types. For instance, 194 lifetime determination can be made using more complex boards or GaN switches by verifying that the 195 complexity does not mask the acceleration of relevant failure mechanisms. Conversely simpler boards 196 can be used to assure application-use reliability by providing collateral material showing robustness to 197 operating modes not tested. 198

- The core of this guideline is organized into four clauses, with clauses 5-7 reflective of the aspects of Figure 1.
- Clause 4 gives general guidance for selecting test devices, test circuits and developing test plans.
- 203 Clause 5 provides an approach for broad coverage by using the switching locus curve.
- 204 Clause 6 gives the procedure for obtaining wearout models and device lifetime.
- Finally, clause 7 provides guidance on validating reliable operation of GaN switches in
 power conversion applications.
- 207

1 Scope 208

This publication presents guidelines for evaluating the switching reliability of GaN power 209 switches. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power 210 solutions and cascode GaN power switches. It covers the following aspects: 211

- a) An approach for broad coverage, using the switching locus to represent switching stress in 212 a standardized manner. 213
- b) The development of a lifetime model, based upon the type of application switching locus. 214
- c) The validation of reliable operation under application-use conditions. 215
- The publication will result in common methods for representing, evaluating and modeling the 216 switching stress on GaN power switches, and ensuring their reliable operation in an 217 218 application.

2 Normative references 219

- 220 JEDEC JEP173, Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power 221 Conversion Devices, Version 1.0, January 2019
- To add: upon publication: IEC 63284 ED1, Semiconductor devices Reliability test method by inductive 222 load switching for gallium nitride transistors 223
- Terms, definitions, symbols and abbreviated terms 3 224
- No terms and definitions are listed in this document ISO and IEC maintain terminological 225 databases for use in standardization at the following addresses: 226
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Symbol or Abbreviation_4	Name or term					
Rds(ON)	Drain to Source Resistance of DUT in ON-state					
VT	Threshold Voltage					
İD	Drain current of the DUT, time varying					
VDS	Drain to Source Voltage of DUT, time varying					
ID	Drain current in on-state of DUT					
V _{DS}	Drain to Source Voltage of DUT					
IDP	Drain current parameter to represent the switching stress					
Vdp	Drain voltage parameter to represent the switching stress					
MTTF	Mean Time To Failure for a set of stress conditions					
ttf	Times To Failure					
E _A	Activation Energy					
TJ	Junction Temperature of DUT					
Tc	Case Temperature of DUT					
R _{θJC}	Thermal resistance from device junction to case					
fsw	Switching Frequency					
D	Duty cycle					
tr	Rise Time of VDS while switching					
t _f	Fall Time of VDS while switching					

Symbol or Abbreviation	Name or term
fv, i, T, etc	Acceleration function for given stressor
AF	Acceleration Factor
K1, K2, K3, K4	Constants in empirical acceleration models
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
FET	Field Effect Transistor
HTOL	High Temperature Operating Life
UIS	Unclamped Inductive Switching
HCI	Hot Carrier Injection
DOE	Design of Experiments
SALT	Switching Accelerated Life Test
DHTOL	Dynamic High Temperature Operating Life
DUT	Device Under Test
PCB	Printed Circuit Board
HTRB	High Temperature Reverse Bias
ZCS	Zero Current Switched
ZVS	Zero Voltage Switched DARD

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Description of test elements **REVIEW** 4 231

Objectives of stress testing for switching reliability 4.1 232

There are two classes of stress tests recommended in this guideline: Switching Accelerated 233 Life Test (Switching-ALT or SALT) and Dynamic High-Temperature Operating-Life (DHTOL) 234 test. oSIST prEN IEC 63419:2022 235

For an accelerated lifetime test such as SALJ, stress conditions are typically chosen such that

236 there will be wearout failures in the test timeframe. Failures are needed to allow the plotting of 237 failure distributions, e.g., Weibull, lognormat Oetc. Wearout models are obtained using these 238 distributions and allow calculation of the device lifetime for application-use conditions. Further 239 details about lifetime determination using SALT are provided in clause 6. 240

For DHTOL, stress conditions are chosen to represent the most stringent mission profile so as 241 to cover all different application use cases, as described further in clauses 5 and 7. DHTOL 242 conditions are typically not chosen to stress till wearout, and it is expected that there will be no 243 failures in the test timeframe. Industry best-practice conditions are used in cases where GaN-244 specific knowledge is not yet available. An example of best-practice conditions in use for 245 silicon discrete power FETs is the application of stress at 80% of the device rating (or absolute 246 maximum voltage), or at 100% of the maximum recommended voltage (if specified) and the 247 maximum recommended temperature for 1000h. 248