

# SLOVENSKI STANDARD oSIST prEN IEC 60747-15:2023

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Polprevodniški elementi - 15. del: Diskretni elementi - Izolirani močnostni polprevodniški elementi
Semiconductor devices - Part 15: Discrete devices - Isolated power semiconductor devices
Halbleiterbauelemente - Einzel-Halbleiterbauelemente - Teil 15: Isolierte Leistungshalbleiter
Dispositifs à semiconducteurs - Partie 15: Dispositifs discrets - Dispositifs de puissance à semiconducteurs isolés
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31.080.01 Polprevodniški elementi (naprave) na splošno

Semiconductor devices in general

oSIST prEN IEC 60747-15:2023

en

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# 47E/812/CDV

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SECRETARIAT:		SECRETARY:	
Korea, Republic of		Mr Hojun Ryu	
OF INTEREST TO THE FOLLOW	ING COMMITTEES:	PROPOSED HORIZONTAL STA	NDARD:
		Other TC/SCs are requested any, in this CDV to the sec	ed to indicate their interest, if retary.
FUNCTIONS CONCERNED:			
□ EMC		QUALITY ASSURANCE	SAFETY
	C PARALLEL VOTING		NELEC PARALLEL VOTING
Attention IEC-CENELEC pa	arallel voting		
The attention of IEC Nation CENELEC, is drawn to the fa for Vote (CDV) is submitted	al Committees, members of act that this Committee Draft for parallel voting.	60747-15:2023	
https://standa	rds.iteh.ai/catalog/stand	ards/sist/81594492-c92	
CENELEC online voting sys	e invited to vote through the tem.		

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### TITLE:

Semiconductor devices - Part 15: Discrete devices - Isolated power semiconductor devices

PROPOSED STABILITY DATE: 2029

NOTE FROM TC/SC OFFICERS:

The order of titles is changed for consistency with other IEC 60747 series.

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137	Part 15: Discrete devices -	<ul> <li>Isolated power se</li> </ul>	miconductor devices
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180 181	This third edition cancels and replace constitutes a technical revision.	es the second edition	published in 2010. This edition
182 183	This edition includes the following signedition:	nificant technical chang	es with respect to the previous
184 185	<ul> <li>a) The intelligent power semiconductor the first and second edition, is now</li> </ul>	or modules (IPM), whic included in this docume	h was previously excluded from ent (Annex C);
186	b) The thermal resistance is described	I for each switch (6.2.4)	1

c) Added isolation test between temperature sensor and terminals, in case there is an agreement with the user (6.1.2).

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189 The text of this International Standard is based on the following documents:

Draft	Report on voting
47E/XX/FDIS	47E/XX/RVD

190

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

193 The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members\_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

198 This International Standard is to be used in conjunction with IEC 60747-1:2006 and 199 Amendment 1: 2010.

A list of all parts in the IEC 60747 series, published under the general title *Semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
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- 210

211 SEMICONDUCTOR DEVICES –
 212
 213 Part 15: Discrete devices – Isolated power semiconductor devices
 214
 215

#### 216 **1 Scope**

This part of IEC 60747 gives the requirements for isolated power semiconductor devices. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices and parts of IEC 60748 for ICs.

#### 220 **2** Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60270:2015, High-voltage test techniques – Partial discharge measurements

IEC 60664-1:2020, Insulation coordination for equipment within low-voltage systems – Part 1:
 Principles, requirements and tests

IEC 60721-3-3:2019, Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations

231 IEC 60747-1:2010, Semiconductor devices – Part 1: General 23 https://standards.iteh.ai/catalog/standards/sist/81594492-c923-4b42-bcb4-

- IEC 60747-2:2016, Semiconductor devices Discrete devices and integrated circuits Part 2:
   Rectifier diodes
- IEC 60747-6:2016, Semiconductor devices Part 6: Thyristors
- IEC 60747-7:2019, Semiconductor discrete devices and integrated circuits Part 7: Bipolar
   transistors
- IEC 60747-8:2021, Semiconductor devices Part 8: Field-effect transistors
- IEC 60747-9:2019, Semiconductor devices Discrete devices Part 9: Insulated-gate bipolar
   transistors (IGBTs)
- IEC 60749-5:2017, Semiconductor devices Mechanical and climatic test methods Part 5:
   Steady-state temperature humidity bias life test
- IEC 60749-6:2017, Semiconductor devices Mechanical and climatic test methods Part 6:
   Storage at high temperature
- IEC 60749-10:2003, Semiconductor devices Mechanical and climatic test methods Part 10:
   Mechanical shock
- IEC 60749-12:2017, Semiconductor devices Mechanical and climatic test methods Part 12:
   Vibration, variable frequency

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- IEC 60749-15:2020, Semiconductor devices Mechanical and climatic test methods Part 15: 248 Resistance to soldering temperature for through-hole mounted devices 249
- IEC 60749-21:2011, Semiconductor devices Mechanical and climatic test methods Part 21: 250 Solderability 251
- IEC 60749-25:2003, Semiconductor devices Mechanical and climatic test methods Part 25: 252 Temperature cycling 253
- 254 IEC 60749-34:2010, Semiconductor devices – Mechanical and climatic test methods – Part 34: 255 Power cycling

#### **Terms and definitions** 3 256

- For the purposes of this document, the following terms and definitions apply. 257
- 258 ISO and IEC maintain terminology databases for use in standardization at the following addresses: 259
- IEC Electropedia: available at https://www.electropedia.org/ 260 •
- ISO Online browsing platform: available at https://www.iso.org/obp 261 •

#### 3.1 262

#### isolated power semiconductor device 263

semiconductor power device that contains an integral electrical insulator between the cooling 264 surface or base plate and any isolated circuit elements 265

266 3.2

#### Constituent parts of the isolated power semiconductor device 267

3.2.1

- 268 switch 269
- any single component that performs a switching function in a electrical circuit, e.g. diode, 270 thyristor, MOSFET, etc. 271
- 272 Note 1 to entry: A switch might be a parallel or series connection of several chips with a single functionality.
- 3.2.2 273

#### base plate 274

part of the package having a cooling surface that transfers the heat from inside to outside 275

#### 3.2.3 276

- main terminal 277
- terminal having a high potential of the power circuit and carrying the main current. The main 278 terminal can comprise more than one physical connector. 279

#### 3.2.4 280

#### 281 control terminal

terminal having a low current capability for the purpose of control function, to which the external 282 control signals are applied or from which sensing parameters are taken 283

#### 3.2.4.1 284

#### high voltage control terminal 285

terminal electrically connected to an isolated circuit element, but carrying only low current for 286 control function 287

288 Note 1 to entry: Examples include current shunts and collector sense terminals having the high potential of the main 289 terminals.

#### 3.2.4.2 290

#### low voltage control terminal 291

- terminal having a control function and isolated from the high voltage control terminals 292
- Note 1 to entry: Examples include the terminals of isolated temperature sensors and isolated gate driver inputs etc. 293
- 3.2.5 294

#### 295 insulation layer

296 integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element 297

#### 3.3 298

#### peak case non-rupture current 299

peak current, which will not lead to a rupture of the package, ejecting plasma and massive 300 particles under specified conditions 301

#### 3.4 302

#### thermal interface material 303

heat conducting material between base plate and external heat sink 304

#### Letter symbols 305 4

- 4.1 General 306
- General letter symbols are defined in Clause 4 of IEC 60747-1:2010. 307

#### Additional subscripts/symbols 308 4.2

- p = parasitic 309
- t = terminal 310

312

isol = isolation 311

List letter symbols 0647a80db8/osist-pren-iec-60747-15-2023 4.3

#### 313 4.3.1 Voltages and currents

Terminal current	$I_{\mathrm{tRMS}}$
Isolation voltage	$V_{\sf isol}$
Partial discharge inception voltage	V <sub>i</sub>
Partial discharge extinction voltage	$V_{e}$
Isolation leakage current	$I_{\rm isol}$

#### 4.3.2 **Mechanical symbols** 314

Mounting torque for screws to heat sink	$M_{\rm s}$
Mounting torque for terminal screws	$M_{t}$
Mounting force	F
Maximum acceleration in all 3 axis (x, y, z)	а
Mass	т
Flatness of the case (base-plate)	$e_{\rm c}$
Flatness of the cooling surface (heat sink)	$e_{s}$
Roughness of the case (base plate)	$R_{\sf Zc}$
Roughness of the cooling surface (heat sink)	R <sub>Zs</sub>

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d<sub>(c-s)</sub>

Thickness of thermal interface material (case - sink)

#### **4.3.3 Other symbols**

Parasitic inductance, effective between terminals and chips (to be specified)	$L_{p}$
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	$C_{p}$
Lead resistance between terminal x and internal device connection x'	r <sub>xx</sub> ,
Terminal temperature	T <sub>t</sub>
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

316

### **5** Essential ratings (limiting values) and characteristics

#### 318 5.1 General

Isolated power semiconductor devices should be specified as case rated or heat-sink rated
 devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another
 specified elevated temperature. Requirements for multiple devices having a common
 encapsulation are described in 5.12 of IEC 60747-1:2010.

#### 323 5.2 Ratings (limiting values)

# 5.2.1 Isolation voltage or Isolation test voltage ( $V_{isol}$ )

Maximum RMS or DC value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time.

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### **5.2.2 Peak case non-rupture current (where appropriate)**

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles.

### **5.2.3** Terminal current (*I*<sub>tRMS</sub>) (where appropriate),

Maximum RMS value of the current through the main terminal under specified conditions at minimum mounting torque  $M_t$  and maximum allowed terminal temperature ( $T_{tmax} = T_{stg}$  or  $T_{tmax}$  $\leq T_{vimax}$ ).

#### 335 **5.2.4 Temperatures**

## **5.2.4.1** Solder temperature (*T*<sub>sold</sub>) (where appropriate)

Maximum solder temperature  $T_{sold}$  during solder process over a specified solder processing time  $t_{sold}$ .

## 339 5.2.4.2 Storage temperature (T<sub>sta</sub>)

340 Minimum and maximum storage temperature.

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#### 341 **5.2.5 Mechanical ratings**

#### 342 5.2.5.1 Mounting torque of screws to heat sink $(M_s)$

Minimum mounting torque that shall be applied to the fixing screws to the heat sink.

### 344 5.2.5.2 Mounting torque of screws to terminals $(M_t)$

Minimum mounting torque that shall be applied to screwed terminals.

#### 346 **5.2.5.3** Mounting force (*F*)

Minimum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device.

#### 349 5.2.5.4 Terminal pull-out force $(F_{t})$

350 Maximum force.

#### 351 **5.2.5.5** Acceleration (*a*)

352 Maximum value along each axis (x, y, z).

### **5.2.5.6** Flatness of the heatsink surface $(e_s)$ (where appropriate)

354 Maximum deviation from flatness for the heatsink surface over the whole mounting area.

### 355 5.2.5.7 Roughness of the heatsink surface $(R_{ZS})$ (where appropriate)

- 356 Maximum roughness of the heatsink surface over the whole mounting area.
- 357 5.2.6 Climatic ratings (where appropriate) rds/sist/81594492-c923-4b42-bcb4-
- a10647a80db8/osist-pren-iec-60747-15-2023
- Limiting values of environmental parameters for the final application as follows.
- 359 ambient temperature
- 360 humidity
- 361 speed and pressure of air
- 362 irradiation by sun and other heat sources
- 363 mechanical active substances
- 364 chemically active substances
- 365 biological issues
- shall be described in classes as specified in IEC 60721-3-3:2019, Table 1.

#### 367 **5.3 Characteristics**

### 368 5.3.1 Mechanical characteristics

### 369 5.3.1.1 Creepage distance along surface $(d_s)$

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112:2020 (details to comparative tracking index "CTI") and IEC 60664-1:2020 Subclause 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance

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considerably (details see 60664-1:2020, examples). This is essential, if dust, moisture or dirt starts to cover the
 surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

### **5.3.1.2** Clearance distance in air $(d_a)$

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate.

NOTE For details, see IEC 60664-1:2020, (Subclause 4.6 and Subclause 5.1) which shows typical examples of various shapes of clearance distances.

### 382 5.3.1.3 Mass (*m*) of the device

383 Maximum value excluding accessories (mounting hardware).

### **5.3.1.4** Flatness of the base plate $(e_c)$ (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

### 387 5.3.2 Parasitic inductance (L<sub>p</sub>)

Maximum or typical value between the main terminals of each main current path.

### 389 5.3.3 Parasitic capacitances (C<sub>p</sub>)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

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### 392 5.3.4 Partial discharge inception voltage ( $V_{iM}$ or $V_{i(RMS)}$ ) (where appropriate)

Minimum peak value  $V_{iM}$  or RMS value  $V_{i(RMS)}$  between the isolated terminals and the base plate (details, see IEC 60270:2015).

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### 5.3.5 Partial discharge extinction voltage ( $V_{eM}$ or $V_{e(RMS)}$ ) (where appropriate)

Minimum peak value  $V_{eM}$  or RMS value  $V_{e(RMS)}$  between the isolated terminals and the base plate (for details, see IEC 60270:2015).

### 398 5.3.6 Thermal resistances

### 399 5.3.6.1 Thermal resistance junction to case for case rated devices $(R_{th(i-c)X})$

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

### 402 5.3.6.2 Thermal resistance case to heat sink $(R_{th(c-s)})$ (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device ("module"), when the case is mounted according to manufacturer's mounting instructions.

### 406 **5.3.6.3** Thermal resistance case to heat sink per switch $(R_{th(c-s)X})$ (where 407 appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M) ) of the isolated case rated devices ("module"), when the case is mounted according to the manufacturer's mounting instructions.

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# 412 5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices $(R_{th(i-s)X})$

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

# 416 5.3.6.5 Thermal resistance junction to sensor $(R_{th(j-r)})$ (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor, when the device is mounted according to the manufacturer's mounting instructions.

419 NOTE The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

# 420 5.3.7 Transient thermal impedance ( $Z_{th}$ )

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in Subclause 5.3.6 and shall be specified in one of the following ways.

# 424 6 Measurement methods

# 425 6.1 Verification of isolation voltage rating

# 426 6.1.1 Verification of isolation voltage rating between terminals and base plate ( $V_{isol}$ )

427 – Purpose

Proof of the ability of the isolated power device to withstand the rated isolation voltage.

- 429 Circuit diagram
- 430 See Figure 1 below. <u>oSIST prEN\_IEC\_60747-15:2023</u> https://standards.iteh.ai/catalog/standards/sist/81594492-c923-4b42-bcb



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Figure 1 – Basic circuit diagram for isolation breakdown withstand
voltage test ("high pot test") with V <sub>isol</sub>

### 434 – Circuit description and requirements

- 435 DUT = Device under test
- 436 G = voltage source with high impedance, capable to supply  $V_{isol}$
- 437 S = main switch
- 438 V = voltmeter for  $V_{isol}$