SLOVENSKI STANDARD
oSIST prEN IEC 60747-15:2023

01-oktober-2023

Polprevodniški elementi - 15. del: Diskretni elementi - Izolirani močnostni polprevodniški elementi

Semiconductor devices - Part 15: Discrete devices - Isolated power semiconductor devices

Halbleiterbauelemente - Einzel-Halbleiterbauelemente - Teil 15: Isolierte Leistungshalbleiter

Dispositifs à semiconducteurs - Partie 15: Dispositifs discrets - Dispositifs de puissance à semiconducteurs isolés

Ta slovenski standard je istoveten z: **prEN IEC 60747-15:2023**

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31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

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47E/812/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

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IEC SC 47E : DISCRETE SEMICONDUCTOR DEVICES	
SECRETARIAT: Korea, Republic of	SECRETARY: Mr Hojun Ryu
OF INTEREST TO THE FOLLOWING COMMITTEES:	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.
FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY	
☒ SUBMITTED FOR CENELEC PARALLEL VOTING **Attention IEC-CENELEC parallel voting** The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting. The CENELEC members are invited to vote through the CENELEC online voting system.	☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING

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TITLE:

Semiconductor devices - Part 15: Discrete devices - Isolated power semiconductor devices

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NOTE FROM TC/SC OFFICERS:

The order of titles is changed for consistency with other IEC 60747 series.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES –

Part 15: Discrete devices – Isolated power semiconductor devices

FOREWORD

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IEC 60747-15 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This third edition cancels and replaces the second edition published in 2010. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) The intelligent power semiconductor modules (IPM), which was previously excluded from the first and second edition, is now included in this document (Annex C);
b) The thermal resistance is described for each switch (6.2.4);
c) Added isolation test between temperature sensor and terminals, in case there is an agreement with the user (6.1.2).

189 The text of this International Standard is based on the following documents:

Draft	Report on voting
47E/XX/FDIS	47E/XX/RVD

190
191 Full information on the voting for its approval can be found in the report on voting indicated in
192 the above table.

193 The language used for the development of this International Standard is English.

194 This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in
195 accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available
196 at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are
197 described in greater detail at www.iec.ch/publications.

198 This International Standard is to be used in conjunction with IEC 60747-1:2006 and
199 Amendment 1: 2010.

200 A list of all parts in the IEC 60747 series, published under the general title *Semiconductor*
201 *devices*, can be found on the IEC website.

202 The committee has decided that the contents of this document will remain unchanged until the
203 stability date indicated on the IEC website under webstore.iec.ch in the data related to the
204 specific document. At this date, the document will be

205 • reconfirmed,
206 • withdrawn,
207 • replaced by a revised edition, or
208 • amended.

209

210

SEMICONDUCTOR DEVICES –

Part 15: Discrete devices – Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the requirements for isolated power semiconductor devices. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices and parts of IEC 60748 for ICs.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60270:2015, *High-voltage test techniques – Partial discharge measurements*

IEC 60664-1:2020, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 60721-3-3:2019, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations*

IEC 60747-1:2010, *Semiconductor devices – Part 1: General*

IEC 60747-2:2016, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6:2016, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7:2019, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

IEC 60747-8:2021, *Semiconductor devices – Part 8: Field-effect transistors*

IEC 60747-9:2019, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60749-5:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-15:2020, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-21:2011, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-25:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-34:2010, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
isolated power semiconductor device
semiconductor power device that contains an integral electrical insulator between the cooling surface or base plate and any isolated circuit elements

3.2
Constituent parts of the isolated power semiconductor device

3.2.1
switch
any single component that performs a switching function in a electrical circuit, e.g. diode, thyristor, MOSFET, etc.

Note 1 to entry: A switch might be a parallel or series connection of several chips with a single functionality.

3.2.2
base plate
part of the package having a cooling surface that transfers the heat from inside to outside

3.2.3
main terminal
terminal having a high potential of the power circuit and carrying the main current. The main terminal can comprise more than one physical connector.

3.2.4
control terminal
terminal having a low current capability for the purpose of control function, to which the external control signals are applied or from which sensing parameters are taken

3.2.4.1
high voltage control terminal
terminal electrically connected to an isolated circuit element, but carrying only low current for control function

Note 1 to entry: Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.2
low voltage control terminal
terminal having a control function and isolated from the high voltage control terminals

Note 1 to entry: Examples include the terminals of isolated temperature sensors and isolated gate driver inputs etc.

3.2.5
insulation layer
integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element

3.3
peak case non-rupture current
peak current, which will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

3.4
thermal interface material
heat conducting material between base plate and external heat sink

4 Letter symbols

4.1 General

General letter symbols are defined in Clause 4 of IEC 60747-1:2010.

4.2 Additional subscripts/symbols

p = parasitic

t = terminal

isol = isolation

4.3 List letter symbols

4.3.1 Voltages and currents

Terminal current	I_{tRMS}
Isolation voltage	V_{isol}
Partial discharge inception voltage	V_i
Partial discharge extinction voltage	V_e
Isolation leakage current	I_{isol}

4.3.2 Mechanical symbols

Mounting torque for screws to heat sink	M_s
Mounting torque for terminal screws	M_t
Mounting force	F
Maximum acceleration in all 3 axis (x, y, z)	a
Mass	m
Flatness of the case (base-plate)	e_c
Flatness of the cooling surface (heat sink)	e_s
Roughness of the case (base plate)	R_{Zc}
Roughness of the cooling surface (heat sink)	R_{Zs}

Thickness of thermal interface material (case - sink)	$d_{(c\text{-}s)}$

4.3.3 Other symbols

Parasitic inductance, effective between terminals and chips (to be specified)	L_p
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	C_p
Lead resistance between terminal x and internal device connection x'	$r_{xx'}$
Terminal temperature	T_t
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat-sink rated devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature. Requirements for multiple devices having a common encapsulation are described in 5.12 of IEC 60747-1:2010.

5.2 Ratings (limiting values)

5.2.1 Isolation voltage or Isolation test voltage (V_{isol})

Maximum RMS or DC value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time.

5.2.2 Peak case non-rupture current (where appropriate)

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles.

5.2.3 Terminal current (I_{tRMS}) (where appropriate),

Maximum RMS value of the current through the main terminal under specified conditions at minimum mounting torque M_t and maximum allowed terminal temperature (T_{tmax} = T_{stg} or $T_{tmax} \leq T_{vjmax}$).

5.2.4 Temperatures

5.2.4.1 Solder temperature (T_{sold}) (where appropriate)

Maximum solder temperature T_{sold} during solder process over a specified solder processing time t_{sold}.

5.2.4.2 Storage temperature (T_{stg})

Minimum and maximum storage temperature.

5.2.5 Mechanical ratings

5.2.5.1 Mounting torque of screws to heat sink (M_s)

Minimum mounting torque that shall be applied to the fixing screws to the heat sink.

5.2.5.2 Mounting torque of screws to terminals (M_t)

Minimum mounting torque that shall be applied to screwed terminals.

5.2.5.3 Mounting force (F)

Minimum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device.

5.2.5.4 Terminal pull-out force (F_t)

Maximum force.

5.2.5.5 Acceleration (a)

Maximum value along each axis (x, y, z) .

5.2.5.6 Flatness of the heatsink surface (e_S) (where appropriate)

Maximum deviation from flatness for the heatsink surface over the whole mounting area.

5.2.5.7 Roughness of the heatsink surface (R_{ZS}) (where appropriate)

Maximum roughness of the heatsink surface over the whole mounting area.

5.2.6 Climatic ratings (where appropriate)

Limiting values of environmental parameters for the final application as follows.

- ambient temperature
- humidity
- speed and pressure of air
- irradiation by sun and other heat sources
- mechanical active substances
- chemically active substances
- biological issues

shall be described in classes as specified in IEC 60721-3-3:2019, Table 1.

5.3 Characteristics

5.3.1 Mechanical characteristics

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112:2020 (details to comparative tracking index “CTI”) and IEC 60664-1:2020 Subclause 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance

considerably (details see 60664-1:2020, examples). This is essential, if dust, moisture or dirt starts to cover the surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate.

NOTE For details, see IEC 60664-1:2020, (Subclause 4.6 and Subclause 5.1) which shows typical examples of various shapes of clearance distances.

5.3.1.3 Mass (m) of the device

Maximum value excluding accessories (mounting hardware).

5.3.1.4 Flatness of the base plate (e_c) (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

5.3.2 Parasitic inductance (L_p)

Maximum or typical value between the main terminals of each main current path.

5.3.3 Parasitic capacitances (C_p)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or RMS value $V_{i(RMS)}$ between the isolated terminals and the base plate (details, see IEC 60270:2015).

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or RMS value $V_{e(RMS)}$ between the isolated terminals and the base plate (for details, see IEC 60270:2015).

5.3.6 Thermal resistances

5.3.6.1 Thermal resistance junction to case for case rated devices ($R_{th(j-c)X}$)

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch “X” (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$) (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device (“module”), when the case is mounted according to manufacturer’s mounting instructions.

5.3.6.3 Thermal resistance case to heat sink per switch ($R_{th(c-s)X}$) (where appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch “X” (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices (“module”), when the case is mounted according to the manufacturer’s mounting instructions.

5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices ($R_{th(j-s)X}$)

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

5.3.6.5 Thermal resistance junction to sensor ($R_{th(j-r)}$) (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor, when the device is mounted according to the manufacturer's mounting instructions.

NOTE The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

5.3.7 Transient thermal impedance (Z_{th})

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in Subclause 5.3.6 and shall be specified in one of the following ways.

6 Measurement methods

6.1 Verification of isolation voltage rating

6.1.1 Verification of isolation voltage rating between terminals and base plate (V_{isol})

– **Purpose**

Proof of the ability of the isolated power device to withstand the rated isolation voltage.

– **Circuit diagram**

See Figure 1 below.

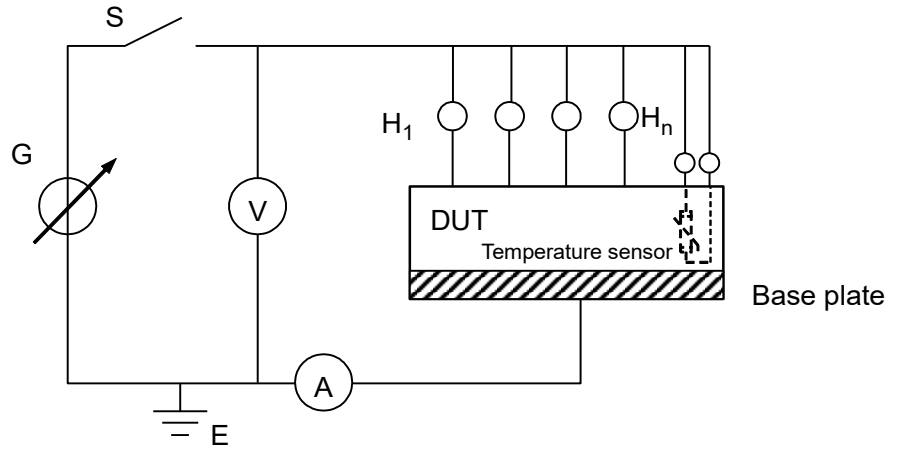

Figure 1 – Basic circuit diagram for isolation breakdown withstand voltage test ("high pot test") with V_{isol}

– **Circuit description and requirements**

DUT = Device under test

G = voltage source with high impedance, capable to supply V_{isol}

S = main switch

V = voltmeter for V_{isol}