SLOVENSKI STANDARD
SIST EN 165000-2:2002

01-september-2002

Film and hybrid integrated - Part 2: Internal visual inspection and special tests

Film and hybrid integrated circuits -- Part 2: Internal visual inspection and special tests

Integrierte Hybrid- und Schichtschaltungen -- Teil 2: Innere Sichtkontrolle und spezielle Prüfungen

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Ta slovenski standard je istoveten z: **EN 165000-2:1996**

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ICS:

31.200	Integrirana vezja, mikroelektronika	Integrated circuits. Microelectronics

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2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

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EUROPEAN STANDARD
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EN 165000-2

April 1996

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Descriptors: **Quality, generic specification, hybrid circuits**

English version

Film and hybrid integrated circuits
Part 2: Internal visual inspection and special tests

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Foreword

This European Standard was prepared by CLC/TC CECC SC 47AX (former CECC/WG 21), Film and hybrid integrated circuits.

The text of the draft was submitted to the Unique Acceptance Procedure and was approved by CENELEC as EN 165000-2 on 1996-03-05.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	1997-03-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	1997-03-01

The present standard, EN 165000-2, Film and hybrid integrated circuits - Part 2: Internal visual inspection and special tests, is intended to be read in conjunction with the other parts of EN 165000, which are:

Part 1: Generic Specification - Capability approval procedure
Part 3: Self-audit checklist and report for film and hybrid integrated circuit manufacturers
Part 4: Customer information, product assessment level schedules and blank detail specification

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Part 3 is primarily intended as a pro-forma for the manufacturer and is not considered *essential* for a customer *in this form*.

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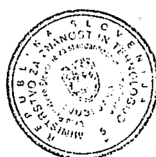
Part 4 is considered an essential document for all users; in particular it includes a helpful introductory section which is aimed at potential customers and seeks to explain the underlying philosophy upon which the whole standard is based.



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SECTION 1 - INTERNAL VISUAL INSPECTION

1 General

1.1 Purpose

The purpose of these examinations is to check the internal materials, added components, construction and workmanship of film and hybrid integrated circuits.

These examinations will normally be used prior to capping or encapsulation to detect and eliminate the circuits with internal defects that could lead to device failure in normal application. Other acceptance criteria may be agreed upon with the purchaser or supplier respectively.

1.2 Sequence of inspection

The sequence which is presented is not a required order of examination and may be varied at the discretion of the manufacturer. Any aspect which may be obscured by a subsequent assembly process shall be examined before that process.

1.3 Inspection apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gauges, drawings, photographs, etc...) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixtures shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

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1.4 Inspection environment

Under consideration.

1.5 Magnification

"High magnification" (100 to 200 x) inspection is normally performed with a microscope perpendicular to the relevant surface with the device under illumination normal to the relevant surface.

"Low magnification" (10 to 100 x) inspection is normally performed with a monocular, a binocular or a stereomicroscope at an appropriate angle and illumination.

1.6 Definitions

1.6.1 Active circuit area

All areas of functional circuit elements, operating metallization or any connected combinations thereof.

1.6.2 Multi-layer metallization (for conductors)

Two or more layers of metal or any other material used for interconnections that are not isolated from each other.

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1.6.3 Edge metallization

Metallization that electrically connects different layers of metallization on or within a substrate at its edge.

1.6.4 Foreign material

Any material not used in the manufacture of the microcircuit or any in-built material that is displaced from its original or intended position within the microcircuit package. Foreign material that appears opaque under those conditions of lighting and magnification used in routine visual inspection shall be considered as conductive.

1.6.5 Protective layer (passivation)

The layer of insulating material that protects part or all of the substrate area, including metallization, but excluding connecting pads, for example glassivation, solder resist, etc...

1.6.6 Isolating layer

A layer used to isolate separate conductive or resistive levels.

1.6.7 Kerf

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The slit or cut made by a material-removing process (for example laser or abrasive trimming).

1.6.8 Multi-level metallization (for conductors)

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Two or more levels of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material and interconnected for example by vias or edge metallization.

1.6.9 Bond pad area

That area of exposed metallization which is not covered by passivation.

1.6.10 Compound bond

Bonding of one bond on top of another bond

1.6.11 Through hole metallization

Metallization that electrically connects different levels of metallization on or within a substrate via a hole or holes.

1.6.12 Scratch

Any tearing defect in the surface of a layer.

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1.6.13 Cosmetic scratch

A shallow scratch which may extend completely across a layer and which does not expose or damage underlying layers, or laterally displace metallization beyond the edge of the conductor for example by mechanical deformation.

1.6.14 Void

Any defect in a layer not caused by a scratch where underlying material is visible.

1.7 Interpretation

Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present.

This shall not require confirmation by any other method of testing.

1.8 Alternative test methods

The visual examination requirements given below are not necessarily the only methods which can be used.

However the manufacturer shall satisfy the ONS that any alternative method will give equivalent assurance otherwise the specified method shall be used.

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2 Substrate and processes

Low magnification

2.1 Substrate

No device shall be acceptable that shows the following:

- Holes through the substrate, except through lead holes, used or unused component mounting holes, or alignment holes.

- Any crack that exceeds 0,125mm in length and points toward an operating portion of the circuit - see fig.1.

- Any chip-out that reduces any active (metallized) circuit area - see fig. 2.

- Any crack that comes closer than 0,025 mm to an operating portion of the circuit - see fig. 3.

- Any substrate having attached portions of another substrate that exceed the substrate dimensions allowed by the assembly drawing - see fig. 4.

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- Any substrate having a section broken out around any substrate mounting hole greater than 25 % of the mounting hole circumference when designed for substrate to post attachment - see fig. 5.

- Any crack that originates at an edge - see fig.6.

2.2 Processes

2.2.1 Conductors

No device shall be acceptable that shows the following:

1) Metallization scratches

A scratch is any tearing effect, including probe marks, in the surface of the metallization.

- Scratch in the metallization excluding bonding pads that exposes the substrate or underlying dielectric anywhere along its length and leaves less than 50 % of the metal width undisturbed - see fig. 7.

- Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 50 % of the top layer metal width undisturbed - see fig. 8.

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- Scratch in the bonding pad or fillet area that exposes the underlying dielectric or substrate and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately - see fig.9.

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2) Metallization voids

- Void(s) in the metallization except for wire or beam lead bonding pads that leaves less than 50 % of the metal width undisturbed - see fig. 7.

- Void(s) in the wire or beam lead bonding pad area that leaves an area less than twice the maximum allowable bond size undisturbed.

- Void(s) in the wire or beam lead bonding pad, including fillet area, that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width - see fig. 9.

NOTE: If two or more stripes enter a bonding pad, each shall be considered separately.

3) Metallization corrosion

Any metallization corrosion - see fig. 10.

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4) Metallization adherence

Any metallization lifting, peeling or blistering - see fig.11.

5) Metallization proving

Criteria contained in 1) and 2) shall apply as limitations on probing damage.

6) Metallization bridging

A protrusion or expansion of the conductor that reduces the existing separation from another element to less than 25 % or to less than 50 % of the minimum insulation distance specified in the design rules, whichever is the greater - see fig. 12.

7) Metallization alignment

Misalignment where the conductor overlap is less than 50 % of the width of the narrower conductor - see fig.13.

2.2.2 Isolating layer

No device shall be acceptable that shows the following:

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- A scratch or void at or over an isolating step - see fig. 15.
- Any misalignment in cross-overs where the dielectric is not visible on each side more than 50 % of the minimum designed insulation distance between circuit elements - see fig. 16.

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- Scratches, nicks or voids that expose the buried conductor - see fig. 17.
- Blistering or crazing - see fig. 18.
- Any dielectric material covering more than 25 % of a bonding or soldering area - see fig. 19.
- Permanent particle or foreign material with any dimension greater than 50 % of the buried element width - see fig. 20.

2.2.3 Resistors

2.2.3.1 Untrimmed resistors

No device shall be acceptable that shows the following:

- A scratch, nick or void with any dimension greater than 50 % of the width - see fig. 21.
- Lifting, peeling or blistering - see fig. 22.

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- A protrusion or expansion of the resistor that reduces the existing separation from another element to less than 25 % or to less than 50 % of the minimum insulation distance specified in the design rules, whichever is the greater - see fig. 23.

- A particle of foreign material with any dimension greater than 50 % of the resistor width - see fig. 24. Trimming shall not touch foreign particles.

- Misalignment in the length direction of a resistor/conductor overlap greater than 50 % - see fig. 25.

- Misalignment in the width direction outside the boundaries of the conductor pattern.

- Any sharp change in colour of the resistor material within the resistor/conductor termination.

2.2.3.2 Trimmed resistors

No device shall be acceptable that shows failures as described in 2.2.3.1 or the following:

1) Abrasion trimmed resistors

- The minimum resistor width remaining after trimming shall be 40 % - see fig. 26, except where it can be shown that the maximum current density permitted by the design rules are not exceeded.

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- Width of the termination reduced by more than 50 % - see fig. 27.

- Bridging of the trim-cut - see fig. 28.

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- A scratch, nick or void opposite a trim kerf which reduces the resistors width to 40 % - see fig. 29.

- Micro cracking and ragged edges in the resistor material - see fig. 30.

-Residue of resistor material in the trim-cut - see fig.31.

2) Laser trimmed resistors

- The minimum resistor width remaining after trimming shall be 40 % - see fig. 26, except where it can be shown that the maximum current density permitted by the design rules are not exceeded.

- Bridging of the trim-cut unless required by the design - see fig.32.

- A scratch, nick or void, in combination with a trim in accordance with requirement above on minimum undisturbed resistor width - see fig.33.