SLOVENSKI STANDARD
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01-maj-2024

Monokristalne rezine za površinske zvočnovalovne naprave (SAW) - Specifikacije in merilne metode

Single crystal wafers for surface acoustic wave (SAW) device applications - Specifications and measuring methods

Einkristall-Wafer für Oberflächenwellen-(OFW-)Bauelemente - Festlegungen und Messverfahren

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ICS:

31.140	Piezoelektrične naprave	Piezoelectric devices

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49/1454/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

PROJECT NUMBER:	
IEC 62276 ED4	
DATE OF CIRCULATION: **2024-03-22**	CLOSING DATE FOR VOTING: **2024-05-17**
SUPERSEDES DOCUMENTS: **49/1425/CDV, 49/1448/RVC**	

IEC TC 49 : PIEZOELECTRIC, DIELECTRIC AND ELECTROSTATIC DEVICES AND ASSOCIATED MATERIALS FOR FREQUENCY CONTROL, SELECTION AND DETECTION	
SECRETARIAT: Japan	SECRETARY: Mr Masanobu Okazaki
OF INTEREST TO THE FOLLOWING COMMITTEES:	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary.
FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT	☒ QUALITY ASSURANCE ☐ SAFETY
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TITLE:

Single crystal wafers for surface acoustic wave (SAW) device applications - Specifications and measuring methods

PROPOSED STABILITY DATE: 2027

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136 **SINGLE CRYSTAL WAFERS FOR SURFACE ACOUSTIC WAVE (SAW)**
137 **DEVICE APPLICATIONS – SPECIFICATIONS AND MEASURING METHODS**

138
139
140

141 ## 1 Scope

142 This document applies to the manufacture of synthetic quartz, lithium niobate (LN), lithium
143 tantalate (LT), lithium tetraborate (LBO), and lanthanum gallium silicate (LGS) single crystal
144 wafers intended for use as substrates in the manufacture of surface acoustic wave (SAW) filters
145 and resonators.

146 ## 2 Normative references

147 The following documents are referred to in the text in such a way that some or all of their content
148 constitutes requirements of this document. For dated references, only the edition cited applies.
149 For undated references, the latest edition of the referenced document (including any
150 amendments) applies.

151 IEC 60758:2016, *Synthetic quartz crystal – Specifications and guidelines for use*

152 ISO 2859-1, *Sampling procedures for inspection by attributes – Part 1: Sampling schemes*
153 *indexed by acceptance quality limit (AQL) for lot-by-lot inspection*

154 ## 3 Terms and definitions

155 For the purposes of this document, the following terms and definitions apply.

156 ISO and IEC maintain terminology databases for use in standardization at the following
157 addresses:

158 • IEC Electropedia: available at https://www.electropedia.org/
159 • ISO Online browsing platform: available at https://www.iso.org/obp

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160 ### 3.1 Flatness

161 **3.1.1**
162 **fixed quality area**
163 **FQA**
164 central area of a wafer surface, defined by a nominal edge exclusion, X, over which the specified
165 values of a parameter apply

166 Note 1 to entry: The boundary of the FQA is at all points (e.g. along wafer flats) the distance X away from the
167 perimeter of the wafer of nominal dimensions as shown in Figure 1.

168 **3.1.2**
169 **reference plane**
170 plane used as a reference for flatness measurements

171 Note 1 to entry: The reference plane can be one of the following types:

172 a) for measurements in which the wafer is clamped, the reference plane is the flat chuck surface that is identical
173 with the back surface of the wafer;

174 b) for measurements in which the wafer is not clamped, the reference plane is defined by the surface height at three
175 points on the front surface of the wafer within the FQA;

176 c) for measurements in which the wafer is not clamped, the reference plane is defined by the least-squares fit to
177 the front surface of the wafer using the surface height at all measured points within the FQA.

178 **3.1.3**
179 **site**
180 square area on the front surface of the wafer with one side parallel to the OF

181 Note 1 to entry: Flatness parameters are assessed either globally for the FQA, or for each site individually.

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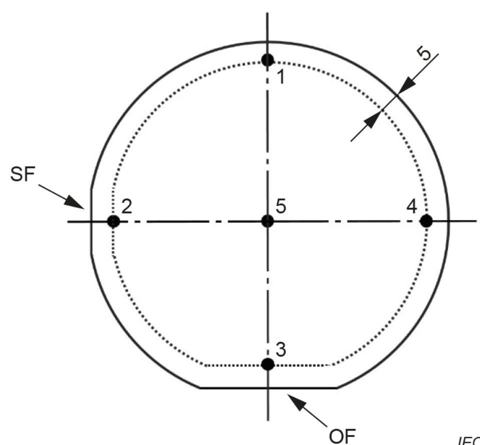
182 **3.1.4**
183 **thickness variation for five points**
184 **TV5**
185 difference between the maximum thickness and the minimum thickness at the centre and four
186 peripheral points of the wafer as shown in Figure 1

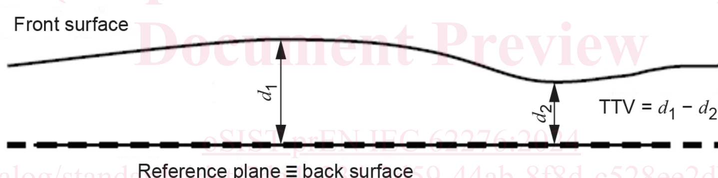
187 Dimensions in millimetres



188

189 **Figure 1 – Wafer sketch and measurement points**

190 **3.1.5**
191 **total thickness variation**
192 **TTV**
193 difference between the maximum thickness d_1 and the minimum thickness d_2 of a wafer as
194 shown in Figure 2



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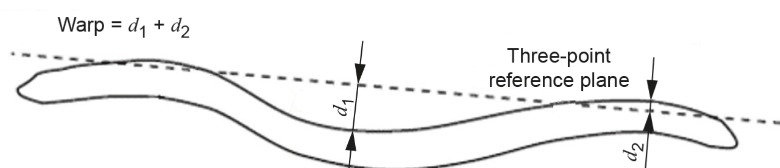
195 IEC

196 **Figure 2 – Schematic diagram of a TTV**

197 Note 1 to entry: Measurement of TTV is performed on a clamped wafer with the reference plane as defined in
198 3.1.2 a).

199 **3.1.6**
200 **warp**
201 maximum distance between the highest point and the lowest point on the front surface of an
202 unclamped wafer from the reference plane, where the three-point reference plane is used



203 IEC

204 **Figure 3 – Schematic diagram of a warp**

205 Note 1 to entry: The warp describes the deformation of a wafer that is not clamped, as shown in Figure 3.

206 Note 2 to entry: The reference plane is defined by the surface height at three points on the front surface of the
207 wafer as described in 3.1.2 b).

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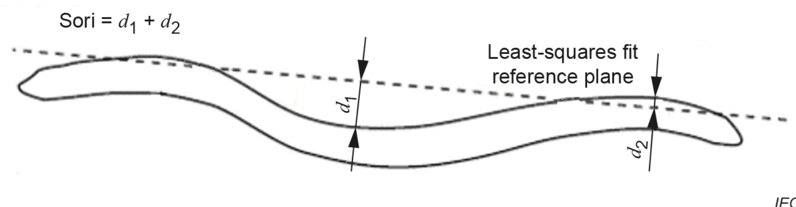
208 **3.1.7**
209 **sori**
210 maximum distance between the highest point and the lowest point on the front surface of an
211 unclamped wafer from the reference plane, where the least-squares fit reference plane is used



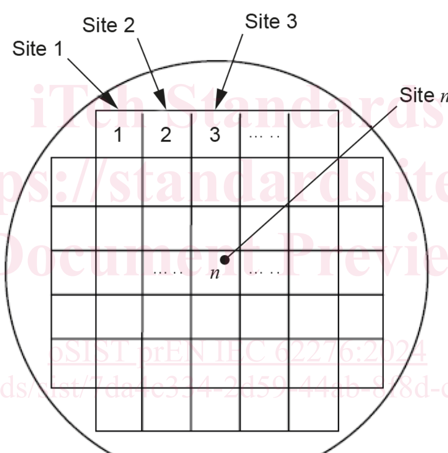
212

213 **Figure 4 – Schematic diagram of a sori**

214 Note 1 to entry: The sori describes the deformation of a wafer that is not clamped, as shown in Figure 4.

215 Note 2 to entry: The reference plane is defined by the least-squares fit to the front surface of the wafer as described
216 in 3.1.2 c).

217 **3.1.8**
218 **local thickness variation**
219 **LTV**
220 difference between the maximum value and the minimum value of a wafer thickness at each
221 site of the wafer surface



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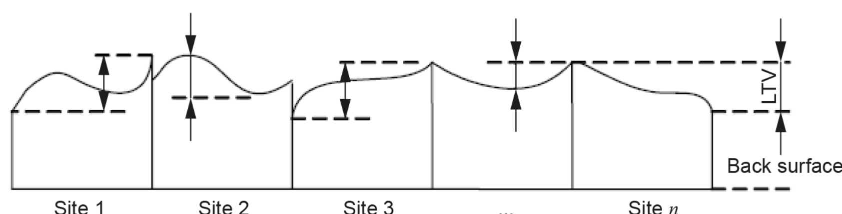
222

223 Note 1 to entry: All sites existing within the fixed quality area (FQA) on the wafer surface possess their own LTV
224 value.

225 **Figure 5 – Example of the distribution of sites for measurement of the LTV**



226

227 **Figure 6 – LTV defined within each site on the wafer surface**

228 Note 2 to entry: Measurement is performed on a clamped wafer with the reference plane as defined in 3.1.2 a). An
229 example of the distribution of sites for measurement of the LTV is shown in Figure 5. The LTV is defined within each
230 site, as illustrated in Figure 6.

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231 **3.1.9**
232 **percent local thickness variation**
233 **PLTV**
234 percentage of sites whose local thickness variation values fall within the specified value

235 Note 1 to entry: As with the LTV, measurement is performed on a clamped wafer with the reference plane defined
236 in 3.1.2 a).

237 **3.1.10**
238 **focal plane deviation**
239 **FPD**
240 maximum distance between a point on the wafer surface within the fixed quality area and the
241 three-point reference plane

242 Note 1 to entry: The three-point reference plane is defined in 3.1.2 b).

243 Note 2 to entry: If the point on the wafer surface is above the three-point reference plane, the FPD is positive. If
244 that point is below the three-point reference plane, the FPD is negative.

245 **3.2 Appearance defects**

246 **3.2.1**
247 **contamination**
248 foreign matter on a surface of wafer which cannot be removed after cleaning

249 **3.2.2**
250 **crack**
251 fracture that extends to the surface of the wafer and that can or cannot penetrate the entire
252 thickness

253 **3.2.3**
254 **scratch**
255 shallow groove or cut below the established plane of the surface, with a length to width ratio
256 greater than 5:1

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257 **3.2.4**
258 **chip**
259 region where material has been removed from the surface or edge of the wafer

260 Note 1 to entry: The size of a chip can be expressed by its maximum radial depth and peripheral chord length.

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261 **3.2.5**
262 **dimple**
263 smooth surface depression larger than 3 mm diameter

264 **3.2.6**
265 **pit**
266 non-removable surface anomaly

267 EXAMPLE A hollow, typically resulting from a bulk defect or faulty manufacturing process.

268 **3.2.7**
269 **orange peel**
270 **pear skin**
271 large-featured, roughened surface visible to the unaided eye under diffuse illumination

272 **3.3 Other terms and definitions**

273 **3.3.1**
274 **manufacturing lot**
275 lot established by agreement between the customer and the supplier

276 **3.3.2**
277 **orientation flat**
278 **OF**
279 flat portion of a wafer perimeter indicating the crystal orientation

280 Note 1 to entry: Generally, the OF corresponds to the SAW propagation direction (see Figure 1).

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281 **3.3.3**
282 **secondary flat**
283 **SF**
284 flat portion of a wafer perimeter shorter than the orientation flat

285 Note 1 to entry: When present, the SF indicates wafer polarity and can serve to distinguish different wafer cuts (see
286 Figure 1).

287 **3.3.4**
288 **back surface roughness**
289 roughness that scatters and suppresses spurious bulk waves at the back surface of a wafer

290 **3.3.5**
291 **surface orientation**
292 crystallographic orientation of the axis perpendicular to the polished surface of the wafer

293 **3.3.6**
294 **description of orientation and SAW propagation**
295 indication of the surface orientation and the SAW propagation direction, separated by the
296 symbol "-"

297 Note 1 to entry: Specification of a 0° orientation is normally omitted.

298 Note 2 to entry: Description of wafer orientation rule is shown in Annex A.

299 **3.3.7**
300 **tolerance of surface orientation**
301 maximum permissible angular deviation of the surface orientation measured by X-ray diffraction
302 from the specified surface orientation

303 **3.3.8**
304 **bevel**
305 slope of the perimeter edge of a wafer

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306 Note 1 to entry: The process of forming a slope is called "bevelling".

307 Note 2 to entry: Machining of the perimeter edge of a wafer can be performed through bevelling or edge rounding.
308 Whereas bevelling produces a flat slope, edge rounding (as the term implies) produces a rounded edge.

309 Note 3 to entry: Both bevelling and edge rounding, and their tolerances, are subject to agreement between the user
310 and the supplier.

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311 **3.3.9**
312 **diameter of wafer**
313 diameter of circular portion of wafer excluding the OF and SF regions

314 **3.3.10**
315 **wafer thickness**
316 thickness measured at the centre of the wafer

317 **3.3.11**
318 **inclusion**
319 foreign material (solid, liquid or vapor) within a piezoelectric crystal, detectable by examination
320 of scattered light

321 **3.3.12**
322 **electrical twins in synthetic quartz wafer**
323 synthetic quartz wafer in which regions with the common Z-axis exist showing a polarity reversal
324 of the electrical X-axis

325 Note 1 to entry: Electrical twins may result from extreme conditions (temperature and pressure, for example) during
326 processing.

327 3.4 Terms and definitions related to LN and LT wafers

328 **3.4.1**
329 **colour difference**
ΔE^{*}_{ab}
330 difference in colour at different parts of the object surface